Nanolink-based thermal devices: integration of ALD TiN thin films

Alfons Groenland

NANOLINK-BASED THERMAL DEVICES: INTEGRATION OF ALD TiN THIN FILMS

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The cover shows an optical micrograph (topview) of Greek Cross shaped four-point structures with buried electrodes (chapter 2) for the electrical characterization of ultrathin ALD TiN layers ('Dead Cow van der Pauws') during the fabrication process after wet chemical etching of the ALD TiN layer stack, showing redeposited photoresist residues of square-shaped contact chain structures (which are located outside the image).

NANOLINK-BASED THERMAL DEVICES:

INTEGRATION OF ALD TiN THIN FILMS

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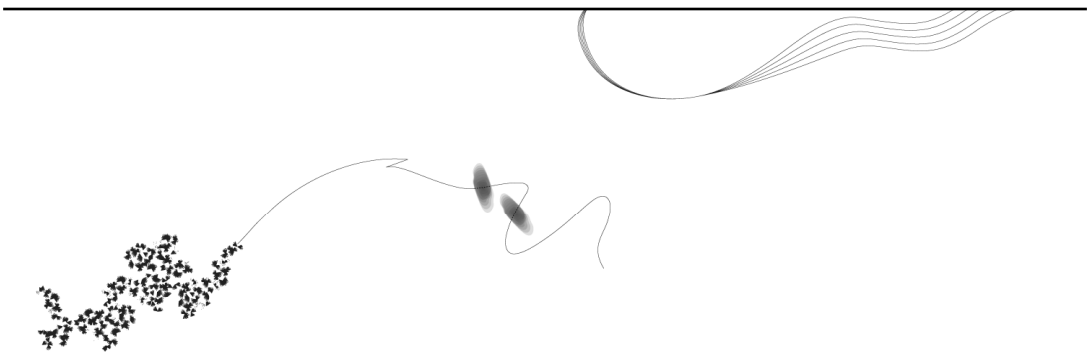
Aan mijn ouders, zus en Femke♥

Contents

1 Introduction



1.1 The Hot Silicon project

"Hot Silicon" is the working title of a project with the official name of "Super Low Power Hot-Surface Silicon Devices for Chemical Sensors and Actuators". The project is funded by the Dutch Technology Foundation (STW), nr. 07682. In this project, the feasibility to realize low-power CMOS-compatible simple and cheap hot surface devices for chemical sensors and actuators is investigated. The Hot Silicon project is a cooperation between two groups within the MESA+ Institute for Nanotechnology: the Semiconductor Components (SC) group, led by prof. dr. J. Schmitz, and the Mesoscale Chemical Systems (MCS) group of prof. dr. J.G.E. Gardeniers.

The work in this thesis has been carried out within the SC group, whereas the integration of devices and the chemistry part in microreactors is studied within the MCS group.

This project is the follow-up of an EU project (GRD1-1999-10849, year 2000-2003) named SAFEGAS (Sensor Arrays for Fast Explosion proof GAS monitoring), in which several ultra low power chemical sensors and actuators were demonstrated [1, 2].

1.2 (Ultra) low power thermal devices

There is a great demand for microelectronic hotplates. Microelectronic hotplates are devices with a surface area of typically 50^2-500^2 μm^2 that can be electrically heated to 100-600 °C with small time constants (~100 μs) and with a power consumption of 20-150 mW [3-5]. Micro hotplates are often used in chemical sensors [6] and mass flow meters [7] based on temperature changes. Because of the elevated operating temperatures, the devices can also be used as chemical actuators, i.e., microreactors providing energy in the form of heat to initiate thermo-activated chemical reactions [8]. Optionally, devices are coated with catalytically active surface coatings to achieve chemical selectivity and/or a lower reaction temperature [9].

Chemical sensors are used for a large variety of applications. These applications include the safety/environment improvement by the detection of

flammable/toxic gases [3] in industrial [10], agricultural [11] or domestic areas [12] as well as at home [13], climate control in buildings or cars [5], process control in industry [5], studying of local chemical kinetics in microreactors [8], laboratory analysis in medical applications [5], and exhaust gas control in aerospace (rockets) [14].

Furthermore, the low power consumption enables battery powered systems with chemical sensors for these applications. Moreover, the low power consumption (10-100 mW) enables systems that can be used for safe detection of flammable gases in dangerous environments (i.e. oilrigs, mines, etc.). Low power systems have no risk of ignition/explosion in case of malfunctioning, and can be operated without the need for an expensive explosion-proof housing, as demanded by European standards [4, 15].

In this work, ultralow power microelectronic hotplates are studied, which have a power consumption of a factor 1000 lower (1-1000 μW) than conventional microelectronic hotplates. This enables the integration of multiple devices in (battery operated) multi-gas sensing arrays [16, 17] or 'electronic noses' [18]. The ultra lower power consumption is primarily achieved by reducing the device dimensions [1, 2, 19], which, together with the ultra low power consumption, enables further integration of chemical sensors in for instance personal digital assistants (PDAs, such as iPhones©, Blackberries©, etc.) or wireless sensor networks [20].

1.2.1 Example: a pellistor

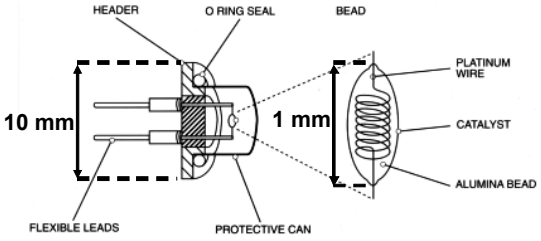
An important example of a micro hotplate device is a gas sensor for hydrocarbons (butane, methane, propane, etc.), the so-called pellistor [5, 9, 11, 16]. Two examples of pellistors are shown in Figure 1.1. This sensor is based on temperature changes due to the catalytic combustion of hydrocarbons. The combustible gas reacts with oxygen on the hot catalytic surface. The catalyst is used to decrease the reaction temperature of for instance oxidation reactions and/or improve selectivity to a certain gas [2, 9, 15]. The catalyst is generally a coating of a transition metal (e.g. platinum (Pt), palladium (Pd) or rhodium (Rh)) on a porous alumina (Al_2O_3) bead or

layer [9, 21, 22]. The porous alumina layer is incorporated to increase the surface area for a higher number of reaction sites and hence more heat generation per unit volume [23]. The heat generated by the combustion process leads to a higher local temperature, which can be detected by a change in the electrical resistance of the heater. In other words, in a pellistor, the microelectronic hotplate simultaneously acts as a thermal actuator to heat the catalytic surface, and as a thermal sensor to monitor the temperature. Both functionalities require a well defined and stable electrical resistance (R) of the heater, and a known temperature coefficient of the resistance (TCR). The catalyst is conventionally incorporated to enable the selective detection of a gas in a mixture, and more importantly, to lower the reaction temperature [24] of the combustion process well below the auto-ignition temperature of the gas mixture [25]. The latter means that the gas is only combusted locally on the catalytic surface, without the risk of explosion of the entire gas volume. This is generally referred to as the 'safe' detection of combustible gases [4].

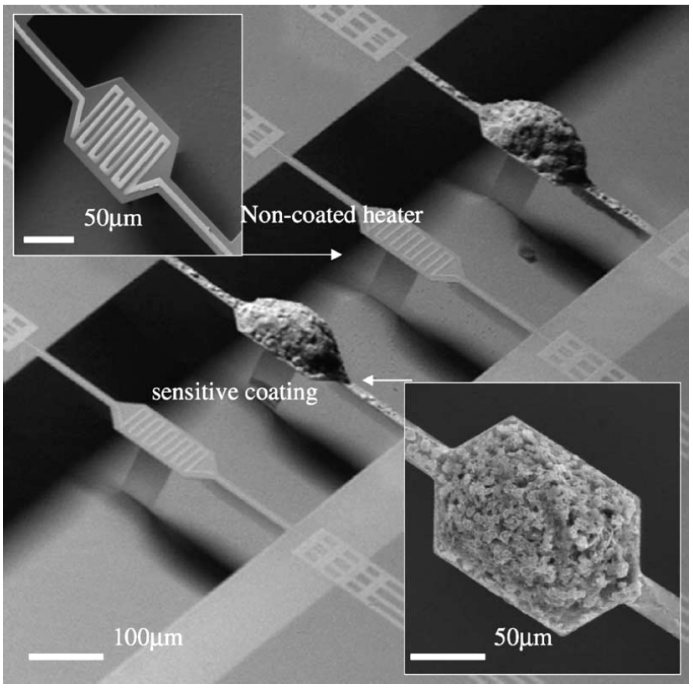
One significant drawback of conventional pellistors is their relatively high power consumption. Commercially available platinum wire-based ('classic') devices (see Figure 1.1a,b) require a power around 200-500 mW [5, 19]. Furthermore, they are difficult to fabricate in a cost effective way as they are made individually [21].

Other types of pellistors, fabricated in the last two decades using microtechnology, are based on a suspended membrane with a platinum thin film resistor (see Figure 1.1c). Although they are a factor 10 smaller than wire-based pellistors, the power consumption is still in the mW range (typically 10-60 mW) [3, 4, 26].

(a)



(b)



(c)

Figure 1.1: Commercially available 'classic' platinum wire based pellistor (by E2V) with a power consumption of typically 100 mW. Housing with and without capping showing the alumina bead (a) and schematic cross-section with the actual pellistor (b), reprinted from [27]. Micromachined pellistor with and without a porous catalytic layer by Ducso et al. with a power consumption of 20-60 mW (c), reprinted from [4].

1.2.2 Anti-fuse based devices

Recently, a new generation of pellistor-type micro hotplate devices, so-called 'suspended membrane actuators' (SMAs), was reported by Kovalgin *et al.* These thermal sensors and actuators have a power consumption of only a few milliwatts [1, 2]. A schematic cross-section of the SMA is shown in Figure 1.2a. The heat is generated by a conductive ***nanolink***: a conductive part with a diameter of 10-100 nm. Situated between two polysilicon electrodes, separated by a thin silicon oxide layer, the nanolink is formed in the so-called 'anti-fuse' process. In this process, a large voltage is applied to the polysilicon electrodes, leading to a high electric field and hence dielectric breakdown of the thin oxide layer. The conductive nanolink, often referred to as the 'anti-fuse' (the term *anti-fuse* means that insulator becomes conductive after fusing, contrary to a conventional *fuse*), is subsequently enlarged, as a result of the applied current stress. Apart from the heating element in pellistors, anti-fuses have found application as the programming element in electrical programmable memories [28-30] and as light emitter [31] or contact electrode [32] in silicon light emitting diodes (LEDs).

In the SMA, heat is generated in the nanolink by forcing a current between pads 1 and 2 (see Figure 1.2b), while the nanolink resistance can be measured (in four-point mode) by measuring the voltage on pads 3 and 4, without the parasitic resistance of the connection wires (R_{con}). Kovalgin *et al.* showed that nanolink-based SMAs can be used as pellistors for the detection of hydrocarbons with a power consumption of only a few mW [2]. In Figure 1.2c, the (nano)link resistance is shown versus time during introduction of butane (C_4H_{10}) pulses into the measurement chamber. The periodic increase in link resistance is due to heating of the nanolink with a positive TCR, as a result of the exothermic combustion reaction of butane on the catalytic surface.

The low power consumption of the nanolink-based SMA is attributed to the high electrical resistance of the link (R_{link}), compared to the resistance of the contact leads (i.e. a high R_{link}/R_{con}-ratio), the minimized heat losses to the substrate as a result of incorporation of a suspended silicon (rich) nitride

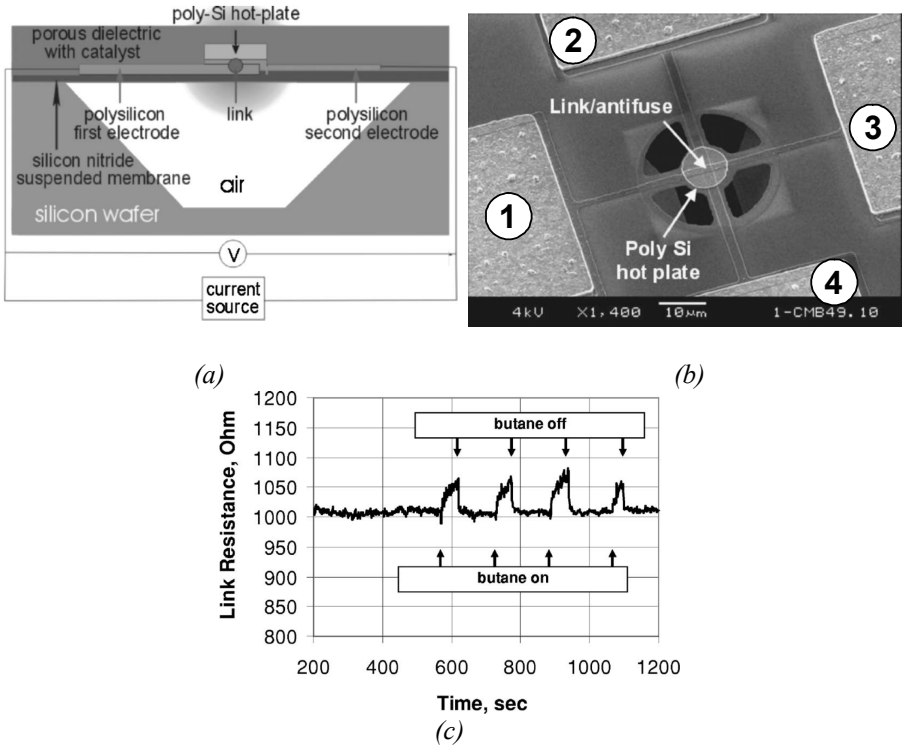


Figure 1.2: Anti-fuse based chemical sensor with nanolink by Kovalgin et al. [2]. Schematic cross-section (a) and SEM topview (b). Numbers refer to the contact pads. Link resistance vs time (c) during the introduction of butane to the measurement chamber. The resistance increases (positive TCR) as butane reacts with oxygen in an exothermic reaction on the catalytic surface. Images reprinted from [2].

(SiRN) membrane and the small device dimensions. The heated area in the device is small compared to other microelectronic heaters with flat meander-shaped platinum heaters [3-5].

1.2.3 Limitations

Although fully functional anti-fuse-based SMAs have been shown, there are some practical limitations. First of all, the positioning of the anti-fuse is not well defined as this is the result of the (statistical) SiO_2 breakdown process. Secondly, the initial electrical characteristics (R_{link}, TCR) are poorly

reproducible. The long term stability of the nanolink is a concern due to the instability of the anti-fuse materials at higher temperature. The individual electrical device programming procedure is time consuming. Furthermore, modeling of the nanolink is difficult because the chemical composition of the antifuse is not well known and it depends on the programming procedure [33, 34].

A serious complication in modeling of the nanolink device is the difference in dimensions within the device: the link is nanoscale, while the device itself is microscale. The thermal and electrical behaviour is described with a different set of equation on micro [5, 35] and nanoscale [36, 37]. This combination and a proper meshing are challenging [38].

1.3 Aim of this work

In this work, we investigate the feasibility of using a new fabrication process for nanolink-based SMAs to overcome the mentioned limitations, and the process has be compatible with standard CMOS processing. The resulting SMA-type microelectronic hotplate devices (in short: SMAs) can be used as pellistor, or for other applications. **The aim is to create the nanolink in a better controlled fabrication process** to achieve better control over the nanolink properties (R_{link} and TCR). They should have a higher long term stability and the devices are programmed by design. CMOS compatible processing improves reproducibility and lowers the fabrication costs. The latter is achieved as many devices are fabricated simultaneously [39]. Furthermore, it allows integration of SMAs with other devices, such as reference sensors [4], control electronics [17] or even a sensor array [3, 16, 40]. Processing should be carried out at temperatures below 450 ºC [41] to enable fabrication of SMAs on top of prefabricated CMOS chips via post-processing [42], for further reduction of the fabrication costs.

The new nanolink-based SMAs are fabricated in a so-called ‘drill-and-fill’ process. This is shown schematically in Figure 1.3. The process includes definition of a nanohole by lithography (Figure 1.3b), etching the hole in an SiO_2 layer on top of the first electrode (Figure 1.3c), and filling of this hole with the second electrode material (Figure 1.3d).

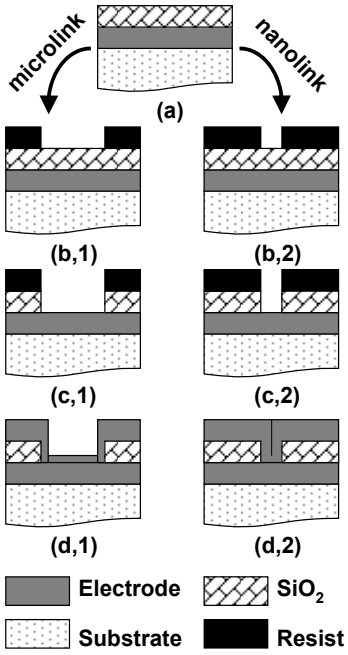


Figure 1.3: 'Drill-and-fill' process for link fabrication: the link is fabricated by first defining a hole by UV ((b,1), for the microlink) or e-beam lithography ((b,2), for the nanolink) on top of the SiO_2 layer covering the bottom electrode. Subsequent etching of the hole in the SiO_2 layer (c) and filling of the hole with a conductive material resulting in a microlink or nanolink (d).

1.3.1 TiN as material for SMAs

In this work, titanium nitride (TiN) is used as material to make the link and the connection electrodes in the 'drill-and-fill' process. TiN is a (conductive) metal nitride known for its high thermodynamic stability, high melting temperature (2950 ºC), high corrosion resistance and it is compatible with the CMOS fabrication processes [43, 44]. It has found applications in IC technology as for example diffusion barrier [45], antireflective coating [46], gate material [47] and current conductor [48]. In MEMS, TiN is used as a heater in micro hotplates [43, 49]. TiN can be deposited via a variety of techniques including physical vapour deposition (PVD) [50], low pressure chemical vapour deposition (LPCVD) [51] and atomic layer deposition

(ALD) [44]. The resistivity depends on the stoichiometry and has a value in the range of 20-575 μΩcm [52, 53]. It has a temperature coefficient of resistance (TCR) in the range of $5\text{-}20\times10^{-4}$ /ºC for sputtered films [54], while for ALD films values of 5.5×10^{-4} /ºC are reported [53]. It can be patterned using wet chemical etching in a hydrogen peroxide-ammonia solution (H_2O_2 + NH_4OH +H_2O [41]) or by plasma etching in a chlorine based plasma [43, 47].

Both PVD and ALD TiN layers are available in the MESA+ Nanolab and can be used for the deposition of thin (100 nm) and ultra-thin (sub 10 nm) films, respectively. Furthermore, both deposition techniques allow the deposition at temperatures compatible with CMOS post-processing (< 450 ºC [41].)

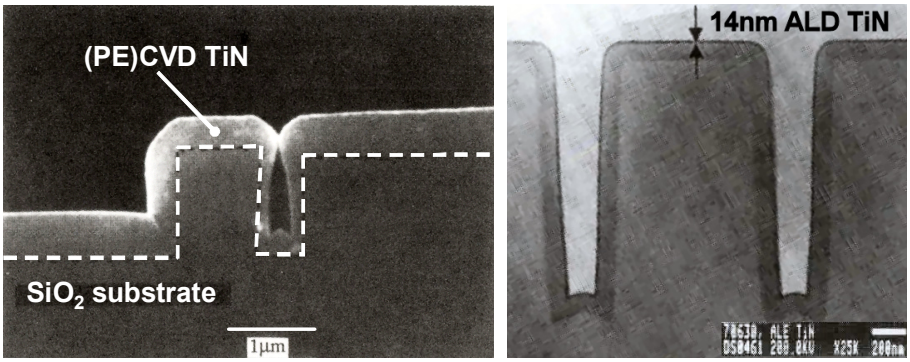
1.3.2 Technological challenges

The 'drill-and-fill' process implies three main technological challenges: definition of the nanoscopic hole by lithography (Figure 1.3b), etching the nanoscopic hole in the SiO_2 layer (Figure 1.3c) and filling the hole with electrode material (Figure 1.3d). In this work, the nanoscopic hole is defined by e-beam lithography, and dry etching of the SiO_2 layer is done in a CHF_3-based plasma. The process can be simplified by the definition of a micron-sized hole in the SiO_2 layer with standard UV lithography. This results in a larger (micro-)link, therefore having a lower link resistance and higher power consumption. The microlink-based SMA is used in this work as a reference device, i.e. for comparison: microlink versus nanolink.

The last challenge is filling the hole with electrode material. Especially for a high aspect ratio hole, it is limited by the step coverage of the deposition process. Conductors are deposited traditionally by physical vapour deposition (PVD) methods, such as sputtering and evaporation. PVD however, cannot be used, due to its poor step coverage [39, 55]. Low temperature chemical vapour deposition (CVD) has a better step coverage (see Figure 1.4a) [51], but the process is difficult to control [56] and more difficult to integrate (i.e. Ti/TiN/W [55]).

Atomic Layer Deposition (ALD) is a CVD-type technique with excellent step coverage (see Figure 1.4b) [57], and is nowadays widely used for the deposition of a variety of materials. ALD is based on deposition cycles of several gas-phase precursors, each cycle results in two self-limiting surface reactions. The precursors are introduced into the reaction chamber subsequently with a long purge time in between, allowing the diffusion of precursors into high aspect ratio holes of micro- [57, 58] and nanosize [59]. In this way, thin films are deposited layer-by-(atomic)-layer, resulting in much lower deposition rates (~5-10 nm/hr) than for conventional CVD (typically a few nm/min or more [39, 60]), but with an excellent step coverage.

In this work the link is fabricated by the deposition of an ultra-thin (7-15 nm) layer of ALD titanium nitride in the etched hole, while the connection electrodes are fabricated from PVD TiN. Furthermore an ALD process is also used for the *in situ* deposition of an Al_2O_3 layer [61] on top of TiN for protection of the ALD TiN thin film.



(a) *(b)*

Figure 1.4: Cross-section SEM micrographs of a titanium nitride (TiN) layer deposited on high aspect ratio structures using (plasma enhanced) chemical vapour deposition (PECVD) (a) and atomic layer deposition (ALD) (b). In (a), the difference in step coverage is shown between a low (left) and high (right) aspect ratio structure. Images reprinted from [55] (a) and [57] (b), respectively.

1.3.3 Thin film deposition equipment

ALD thin films can be deposited, at the MESA+ Institute for Nanotechnology, using the home-built cluster system of the Semiconductor Components group (see Figure 1.5). The system consists of 3 reaction chambers for the deposition of a variety of materials including TiN [62], Al_2O_3 [61] and SiO_2 [63]. The reaction chambers are connected via a shared loadlock which allows wafer transport between the reaction chambers

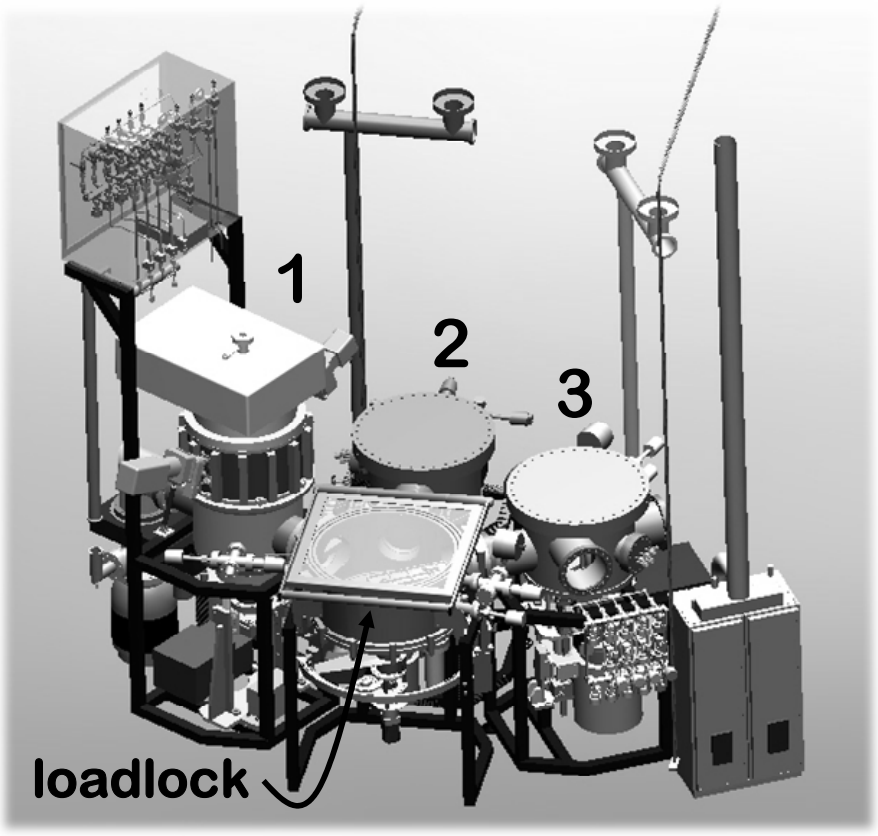


Figure 1.5: Cluster system with three reaction chambers; two reactors are used for the atomic layer deposition of TiN (reactor 2) and Al_2O_3 (reactor 3). In reactor 1, SiO_2 can be deposited at low temperatures (150 ºC) with ICPECVD. All chambers are connected via a shared loadlock, allowing the 'in situ' deposition of multiple layers (without vacuum break).

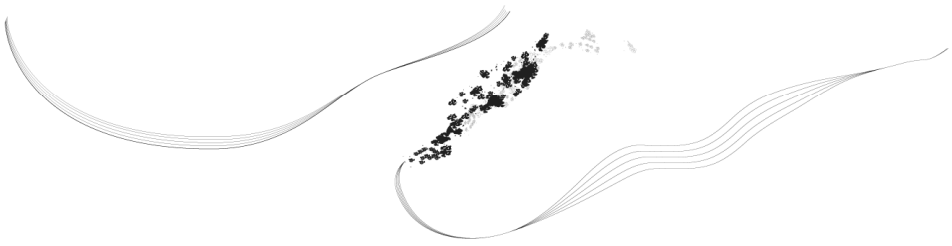
without vacuum break ('*in situ*'). TiN and Al_2O_3 can be deposited via ALD in reactors 2 and 3, respectively. Reactor 1 contains an inductively coupled (IC) plasma source and can be used for the deposition of high quality ICPECVD SiO_2 layers at a temperature as low as 150 ºC [64, 65] and for sputter cleaning (argon bombardment) of surfaces in an argon plasma prior to ALD. Furthermore, a spectroscopic ellipsometer (SE) is mounted on reactor 1 for *in situ* layer thickness measurements [66]. ALD layers deposited in reactor 2 and 3 are characterized after deposition by transferring the wafer into reactor 1.

In this work, all the mentioned methods and materials (ALD of TiN and Al_2O_3, ICPECVD of SiO_2, sputter etching and SE characterization) are used for the fabrication of SMAs.

1.4 Thesis outline

In **chapter 2** the electrical characteristics of thin ALD TiN films are discussed. A novel test structure, aimed for measuring the electrical resistance of ultrathin ALD TiN thin films, is presented. The temperature dependence of the resistance of ALD TiN films is determined up to 700 ºC. In **chapter 3** the stability of ALD TiN films in oxidizing environments (i.e. their oxidation) is investigated, as well as the structural properties (composition, stoichiometry) of as-deposited and oxidized ALD TiN layers. Finally, the quality of different protection (or passivation) layers is discussed. In **chapter 4** the design, fabrication ('drill-and-fill' process) and electrical characterization of micro- and nanolink-based SMAs is presented. In **chapter 5** two alternative techniques for measuring the device temperature (i.e. IR thermometry and polymer melting) are discussed, as well as their applicability to nanolink-based SMAs. In **chapter 6** limitations of the nanolink-based SMAs is presented and related to the process integration of the ALD TiN layer in SMAs. Finally, in **chapter 7** the conclusions of this work are summarized and recommendations for further research are given.

2 The electrical properties of ALD TiN



2.1 Outline

In this work titanium nitride (TiN) is used for the fabrication of a conductive volume (link) in the SMA device using the 'drill and fill' process (section 1.3). The link is fabricated by the deposition of TiN via atomic layer deposition (ALD) in a nanoscopic hole while for the connection electrodes sputtered TiN is used. As the link acts as thermal actuator (heater) and temperature sensor at the same time, the electrical resistance or resistivity (ρ) and its temperature coefficient of resistance (TCR) of the TiN thin film are of prime importance for operation of the SMA device as thermal sensor and actuator. The electrical properties of the TiN films are strongly influenced by the film stoichiometry, crystallinity, morphology, and hence the deposition method [55]. Therefore the electrical properties of ALD TiN films in the thickness range of 4-15 nm are investigated in this chapter.

2.2 Theory of resistivity measurements

2.2.1 Resistivity

The resistance of an arbitrary slab of material (Figure 2.1) is given by

$$R = \rho \frac{L}{Wt} = \rho \frac{L}{A} \qquad (2.1)$$

with R as the resistance [Ω], ρ as the resistivity [Ωcm], as L the length [cm] and W as the width [cm] [67]. The area [cm^2] through which the current flows is A (=w·t). The resistivity is a material parameter and gives the inability of a material to conduct electrical current.

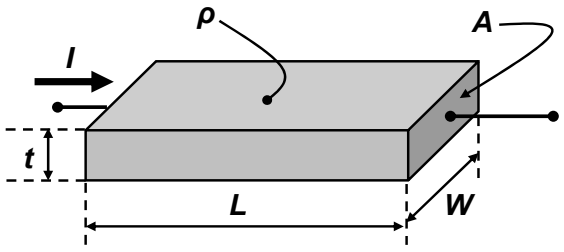


Figure 2.1: Resistor with length L, width W, thickness t, and resistivity ρ, which conducts a current I [67].

Equation (2.1) can be rewritten as

$$R = \frac{\rho}{t}\frac{L}{W} = R_{sh}\frac{L}{W}, \qquad (2.2)$$

with R_{sh} as the sheet resistance in [Ω/□]. The sheet resistance is the ratio between ρ and t:

$$R_{sh} = \frac{\rho}{t} \qquad (2.3)$$

The sheet resistance is commonly used to characterize the resistance of conductive thin films.

2.2.2 Four-point method

The sheet resistance can be obtained from electrical measurements on a conducting thin film using the four-point method and, when the layer thickness is known, the resistivity can be extracted.

The sheet resistance of an arbitrarily shaped object (Figure 2.2) contacted with four probes can be extracted from two resistance measurements [67, 68]. $R_{12,34}$ is obtained when a current (I_{12}) is forced between contacts 1 and 2 and the voltage (V_{34}) is measured between terminals 3 and 4:

$$R_{12,34} = \frac{V_{34}}{I_{12}} \qquad (2.4)$$

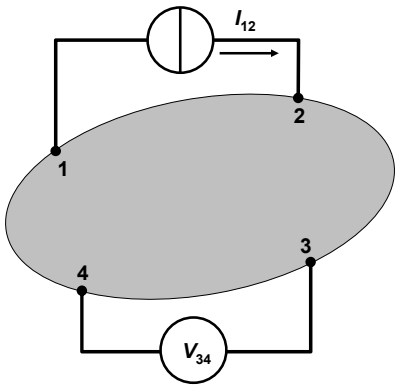


Figure 2.2: Arbitrarily shaped object contacted with four probes to extract the sheet resistance [67, 68]. A current I_{12} is forced between contacts 1 & 2 while the voltage V_{34} is measured between contacts 3 & 4.

Similarly, when the sample is rotated by 90 degrees, the resistance $R_{41,23}$ is defined as

$$R_{41,23} = \frac{V_{23}}{I_{41}}. \qquad (2.5)$$

Van der Pauw [68] showed that, if (*i*) the contacts are sufficiently small (point-like), (*ii*) the sample material is homogeneous in thickness, (*iii*) the contacts are at the circumference of the sample and (*iv*) the surface is singly connected (does not contain isolated holes), then $R_{12,34}$ and $R_{41,23}$ are related by

$$\exp(-R_{12,34}\frac{\pi t}{\rho}) + \exp(-R_{41,23}\frac{\pi t}{\rho}) = 1. \qquad (2.6)$$

This equation can be numerically solved to find ρ:

$$\rho = \frac{\pi}{\ln(2)} t \frac{(R_{12,34} + R_{41,23})}{2} F, \qquad (2.7)$$

where F is a function only of the ratio $R_r = R_{12,34}/R_{41,23}$, satisfying the relation

$$\frac{R_r - 1}{R_r + 1} = \frac{F}{\ln(2)} ar\cosh\left(\frac{\exp[\ln(2)/F]}{2}\right). \qquad (2.8)$$

For symmetrical samples like squares or Greek Crosses, R_r=1 (i.e. $R_{12,34}$=$R_{41,23}$) and F=1, equation (2.7) can be simplified and rewritten to

$$\rho = \frac{\pi}{\ln(2)} t R_{12,34} \approx 4.532 t R_{12,34} \qquad (2.9)$$

or in terms of sheet resistance as

$$R_{sh} = \frac{\rho}{t} = \frac{\pi}{\ln(2)} R_{12,34} \approx 4.532 R_{12,34}. \qquad (2.10)$$

The factor $\pi/\ln(2) \approx 4.532$ is called the correction factor (C_f).

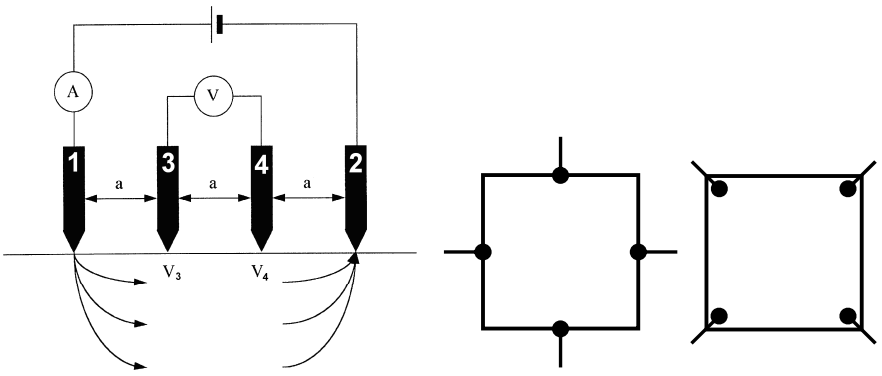
This means the resistivity can be obtained by measuring $R_{12,34}$ and multiplying it with the correction factor, provided the layer thickness is known and the van der Pauw boundary conditions are satisfied.

2.2.3 Four-point test structures

The sheet resistance can be obtained from measurements from large slabs of material using a collinear probe or by measuring $R_{12,34}$ from 'van der Pauw' type test structures. These approaches are described in this section.

2.2.3.1 Collinear probe

The simplest way to measure R_{sh} is to use a four-point probe (FPP) or collinear probe. A FPP consists of four equally spaced in-line-probes which are pressed to a metal thin film. A current is forced between the outer probes (1 and 2) and the voltage is measured across the inner probes (3 and 4) (Figure 2.3a). Similarly to a van der Pauw structure, the standard correction factor of $\pi/\ln(2)$ can be used to obtain R_{sh} provided the sample is 'semi infinite' and the contacts are point-like. This means the current distribution in the thin film is not influenced by the sample edge and the contact area of the probes (i.e. they are sufficiently small). Practically speaking this is the case when the distance between the probes and the sample edge is at least 5 times the distance between two adjacent probes [67]. This method is frequently used to characterize unpatterned conductive thin films or implanted areas during the fabrication process.



(a) *(b)*

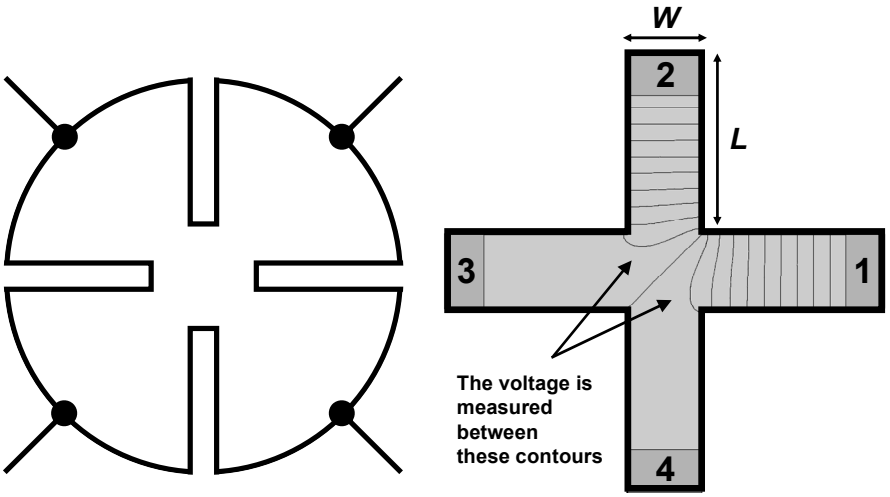
Figure 2.3: Four-point or collinear probe (a) and van der Pauw (vdP) structure (b) for the measurement of the sheet resistance, adapted from [67].

2.2.3.2 Van der Pauw structure

The collinear probe cannot be used for patterned layers to obtain the sheet resistance from small sample areas. Furthermore, it cannot be used for buried layers (e.g. covered with insulating SiO_2/Si_3N_4). Microelectronic test structures are commonly used for these situations [69]. The van der Pauw (vdP) structure is the simplest structure with four contacts at the sample edge. The sheet resistance can be obtained from vdP structures, but often the contacts are not ideal, i.e. they are not small enough ('point-like') or not exactly at the circumference of the sample. Therefore the current distribution in the thin film can be influenced by the contact size and/or position. Hence the correction factor $\pi/\ln(2)$ cannot be used to extract R_{sh} [70]. Correction factors can be obtained via mathematical methods such as conformal mapping in combination with finite element (FE) simulations [71, 72]. These methods are not favourable since they require time intensive calculations.

2.2.3.3 Greek Cross structure

The influence of non ideal contacts can be decreased by making indents in the sample, as in for instance the 'clover leave design' (Figure 2.4a) [72]. A variation on this design is the Greek Cross (GC) structure (Figure 2.4b). Using photolithographic processes, GCs can be made very small and are frequently used for uniformity characterization of conductive thin films during the CMOS fabrication process [67]. When a current is forced between two adjacent contacts, the voltage drop over the central square is measured using the two other contacts. When the arms of the cross are sufficiently long [69, 73, 74], the circular shaped potential distribution around the contacts evolves to straight equipotential lines in the centre of the cross where the voltage is measured. In practice, if $L > 2W$, the size and shape of the contacts do not affect the potential distribution in the centre of the Greek Cross. Greek Crosses with $L > 2W$ fullfil all van der Pauw boundary conditions and the standard correction factor of $\pi/\ln(2)$ can be used to extract R_{sh} [75]. This makes Greek Crosses the prime choice for sheet resistance measurements of thin conducting films.



(a) *(b)*

Figure 2.4: Clover Leaf structure (a) [68] and Greek Cross structure (b) with length (L) and width (W). Lines in the Greek Cross are simulated equipotential lines when a current is forced between contacts 1 and 2, image adapted from [75].

2.2.4 Temperature dependence of resistance

The temperature dependence of the resistance of metals at temperatures > ~20 K originates from electron-phonon scattering [76] and can be described in linear approximation as

$$R = \alpha T + R_0 \qquad (2.11)$$

with R as the resistance [Ω], T as the temperature [ºC] and R_0 as the resistance at 0 ºC [77]. The TCR (or β) can be extracted from the fit parameters α and R_0 by rewriting equation (2.11) as

$$R = R_0(1+\frac{\alpha}{R_0}T) = R_0(1+\beta T), \qquad (2.12)$$

with β defined as

$$\beta = \frac{\alpha}{R_0}. \qquad (2.13)$$

2.3 Special four-point test structures for ultrathin ALD TiN films

2.3.1 Motivation

As shown previously in section 2.2.3, the electrical properties of patterned ALD TiN layers should be measured using van der Pauw or Greek Cross structures. The fabrication of van der Pauw or Greek Cross structures for ultrathin conducting films (sub 10 nm) is challenging. Making electrical contacts to these thin films, using planar technology, is extremely difficult; e.g. etching a via to contact such a film requires a very high selectivity. In practice, this is not possible (Figure 2.5). Enderling and co-workers [78] proposed to use suspended Greek Crosses to overcome this problem. However, this is only suitable for films with a poor step coverage (e.g. deposited via physical vapour deposition (PVD)). Giraudet and co-workers used test structures with predefined metal electrodes for the electrical characterization of thin films with a good step coverage, like spin-coated conducting polymer films [79]. Devices in this work of 'design B' (as will be shown further on in this section) have basically the same architecture.

In this chapter special test structures are presented to measure the electrical properties of ultrathin films in a controlled way without the need of a highly selective SiO_2 to metal etch. These test structures ('design A', see

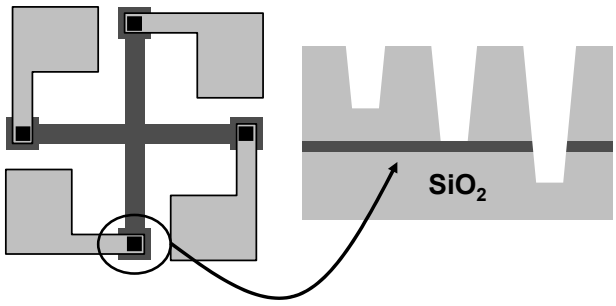


Figure 2.5: Top view of a standard Greek Cross structure (a) with an ultrathin ALD layer. Cross-section of the contact (b) with schematic representation of the via etch for different etching times, illustrating the difficulty to stop exactly at the ALD thin film. This is necessary for a good contact.

Figure 2.6a) can be used generally for thin films, independent of their step coverage. In 'design A', electrodes are fabricated that are buried in a planarized dielectric film. A thin film is deposited on top of the electrodes by means of atomic layer deposition (ALD). The thin film is characterized using the predefined electrode structures, such as the aforementioned vdPs and GCs.

Subsequently, a second set of test structures ('design B', see Figure 2.6b) is fabricated to verify the results obtained from 'design A'. In 'design B', the thin film is deposited directly on top of predefined electrodes without planarization. Due to the (nearly) perfect step coverage of the ALD process, this results in a good electrical contact to the ALD thin film.

'Design A' results in test structures (vdP & GC) with small ('point-like') contacts to the flat ALD thin film, while 'design B' yields (only) GC structures with large contact areas to the ALD thin film following the electrode topography. Test structures in 'design B' are easier to manufacture, they require less process steps and no (difficult) planarization as in 'design A'. However, they cannot be used for very thin films having a poor step coverage such as sputtered or evaporated films. In contrast, the structures of 'design A', are not limited by step coverage.

It is shown that the step coverage of the ALD TiN process is capable of following the topography of structures of 'design B', and hence both test structures can be used successfully for the electrical characterization of ALD thin films.

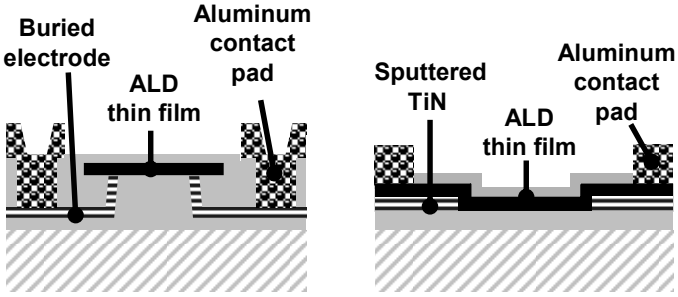


Figure 2.6: Schematic representation (cross-section) of test structures for ultra-thin (ALD) conducting films. 'Design A' (a) and 'design B' (b).

2.3.2 Design & fabrication

2.3.2.1 'Design A'

Oxide pillars are formed by patterning a layer of 0.5 μm thermally grown SiO_2 on top of a standard silicon wafer using wet chemical etching. After an additional oxidation step to insulate the silicon substrate (Figure 2.7a), a layer of 70 nm TiW is sputtered and patterned to make the (buried) electrodes and connections (Figure 2.7b). Subsequently a layer of 1 μm PECVD SiO_2 is deposited (Figure 2.7b) and the structure is planarized using chemical mechanical polishing (CMP) (Figure 2.7c). On this surface the thin ALD TiN film is deposited from titanium tetrachloride ($TiCl_4$) and ammonia (NH_3) at 425 °C in a home built ALD reactor [80]. The ALD TiN layer is passivated by *in situ* ALD Al_2O_3 (16 nm) and *ex situ* PECVD SiO_2 layers (50 nm) (Figure 2.7d). After patterning the ALD TiN and passivation layers (Figure 2.7e) an additional 50 nm PECVD SiO_2 passivation layer is deposited. Next, vias are etched to the buried electrode connections and filled with sputtered aluminium, resulting in contact pads (Figure 2.7f).

Using this process architecture, a variety of vdP and GC structures has been realized. A set of vdP structures was designed with different probe-to-probe spacings (*A*) and with different contact-to-edge-distances (*y*), according to Figure 2.8a.

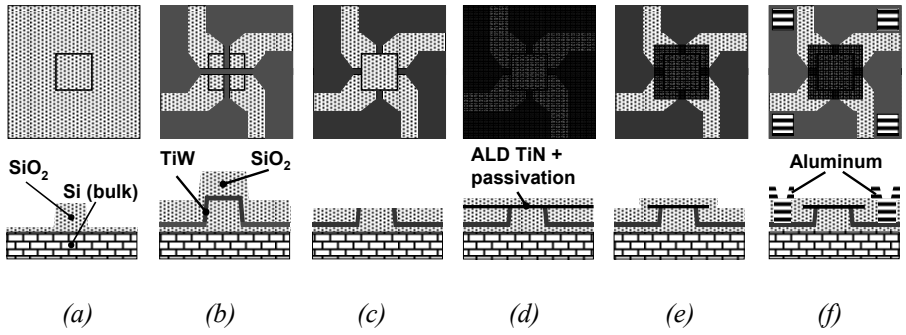
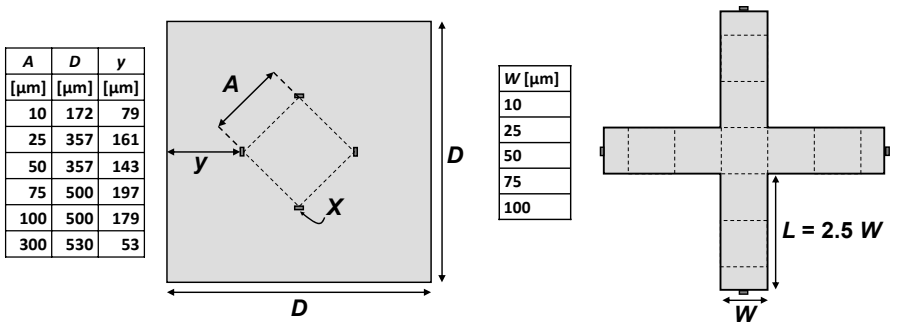


Figure 2.7: 'Process architecture A': fabrication scheme for a van der Pauw structure: (top view (top) and cross-section (bottom))

This was done to account for alignment errors and process variations. Furthermore, a set of GC structures was designed with different *W* values, according to Figure 2.8b. Greek Crosses are designed with the arm length *L* equal to 2.5 times the width *W*. This reduces the error in the extracted sheet resistance to < 1 %, while maintaining maximum sensitivity and minimal Joule heating in the arms of the cross [75]. VdP and GC structures were placed in a die (see Figure 2.9) which was replicated 81 times over a 100 mm wafer. An example of a realized van der Pauw structure is shown in Figure 2.10. A cross-section of the device at the position where the buried TiW electrode contacts the ALD TiN electrode is shown in Figure 2.12. It is observed that the (grainy) ALD TiN layer makes contact with the buried TiW electrode. The width of the contact is estimated at 100 nm.

Using these test structures, 4 and 7 nm ALD TiN layers were electrically characterized.



A [µm]	D [µm]	y [µm]
10	172	79
25	357	161
50	357	143
75	500	197
100	500	179
300	530	53

W [µm]
10
25
50
75
100

(a) *(b)*

Figure 2.8: Schematic design of a van der Pauw (only 'design A') (a) and Greek Cross (b) device ('design A and B'). The four contacts of the van der Pauw are situated at the corners of an imaginary square at a distance A that is centered with respect to the ALD film. The ALD film is patterned as a square with dimension D. X indicates the area of a single contact (2.5 µm×0.1 µm for all devices). The Greek Cross is designed with an arm length L equal to 2.5 times the width W. Dashed lines indicate the (unit) squares.

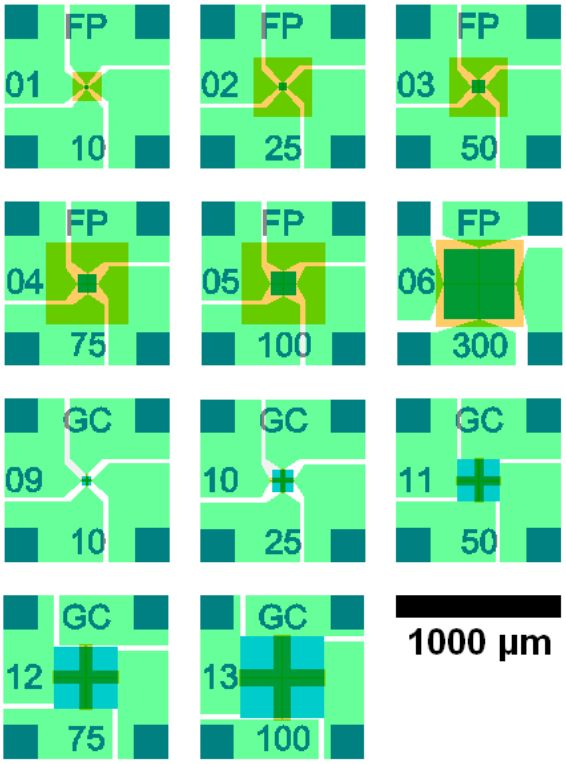
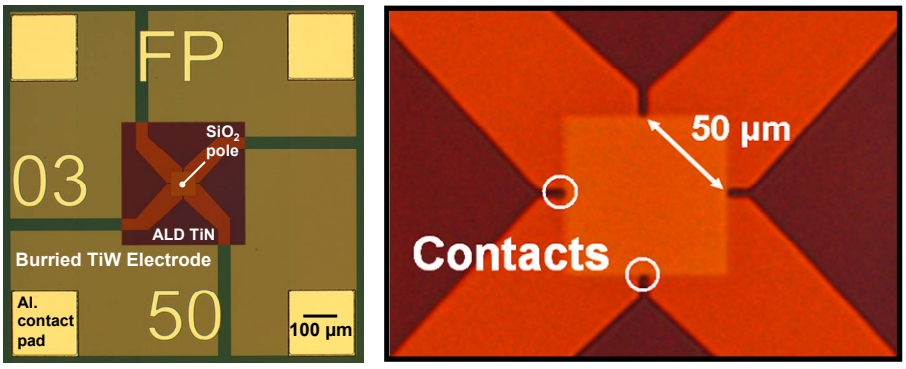
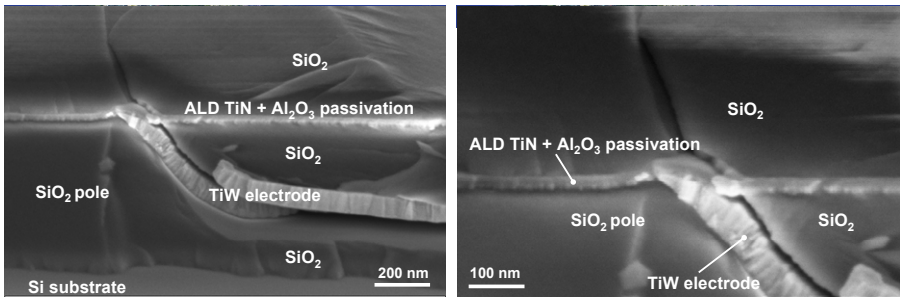


Figure 2.9: Arrangement of vdP (named 'FP') and GC devices in a die of 'design A'. The die is replicated 81 times over a 100 mm wafer.



(a) *(b)*

Figure 2.10: Optical micrograph of a van der Pauw structure ('design A') with a probe-to-probe distance of 50 µm. Complete structure (a) and close-up of the electrodes (b).

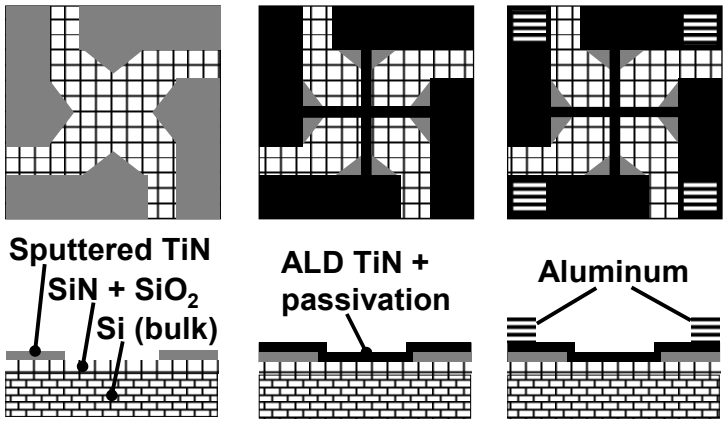


(a) *(b)*

Figure 2.12: Cross-section of the contact of the buried electrode with the ALD TiN layer ('design A'). Overview (a) and close-up (b).

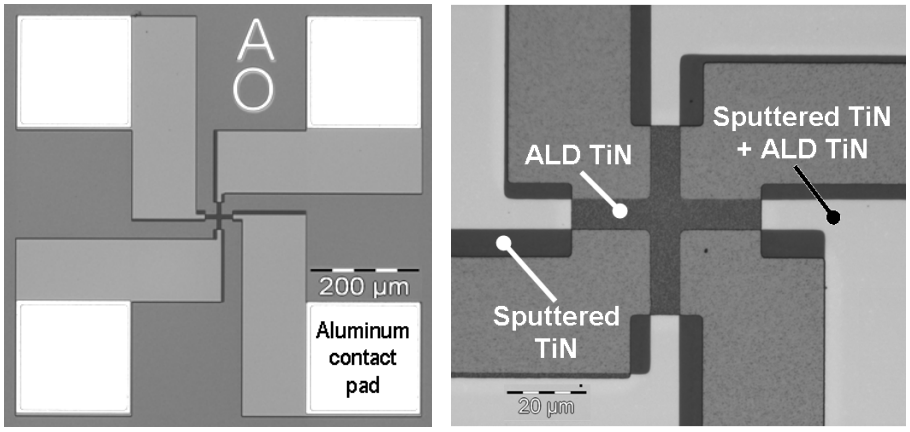
2.3.2.2 'Design B'

A layer of 100 nm TiN is deposited via reactive sputtering of titanium on top of a planar multilayer structure (standard silicon wafer passivated by a layer of 100 nm LPCVD low stress silicon rich nitride (SiRN) and 100 nm PECVD SiO_2). Next, the wafer is annealed by a rapid thermal anneal (RTA) for 30 s at 450 °C in nitrogen (N_2). The TiN layer is patterned using wet chemical etching in a mixture of hydrogen peroxide (H_2O_2) and ammonia (NH_4OH) to define the electrodes (Figure 2.9a). Subsequently, the thin ALD



(a) *(b)* *(c)*

Figure 2.11: 'Design B': fabrication scheme for a Greek Cross structure (top view (top) and cross-section (bottom)).



(a) *(b)*

Figure 2.13: Optical micrograph of an 8 µm Greek Cross structure ('design B'). Whole structure (a) and close up of the centre (b).

TiN film is deposited, which is passivated by *in situ* ALD Al_2O_3 (16 nm) and *ex situ* PECVD SiO_2 (50 nm) layers. After patterning the ALD TiN and passivation layers (Figure 2.9b) an additional 50 nm PECVD SiO_2 passivation layer is deposited. Next, vias are etched in the passivation layer and filled in with sputtered aluminum to become contact pads (Figure 2.9c). This via etch can be carried out without the need for a highly selective SiO_2 to metal etch; the via etch to the ALD TiN layer is terminated in the underlying (thick) TiN electrode without losing electrical contact to the ALD TiN thin film.

In this process architecture, only GC devices with a design similar to 'design A' (Figure 2.8b) with *W*-values of 8 and 50 µm are realized; vdP type are not trivial to be technologically implemented within this process architecture. Both devices are part of a test die which is replicated 44 times over a 100 mm wafer. An example of a realized Greek Cross structure is shown in Figure 2.13.

2.3.3 Experimental

The layer thickness of the ALD TiN films is determined using a Woollam M2000 Spectroscopic Ellipsometer (SE) in the energy range 0.7-5 eV. Measurements were taken *in situ* directly after deposition.

From the recorded SE data, the ALD TiN layer thickness is derived using a model containing the optical constants of all sub-layers which is calibrated against HRSEM measurements [66]. The ALD TiN layer thickness and the contact area of the electrodes are verified by HRSEM on cross-sections of the sample (Figure 2.12).

For the electrical characterization, *IV*-measurements were carried out using a HP4156B or Keithley 4200 precision semiconductor parameter analyser in combination with a Cascade Microtech or Karl Süss PM-8 probe station. For the measurements at elevated temperatures, the temperature controlled chuck of the probe station was used.

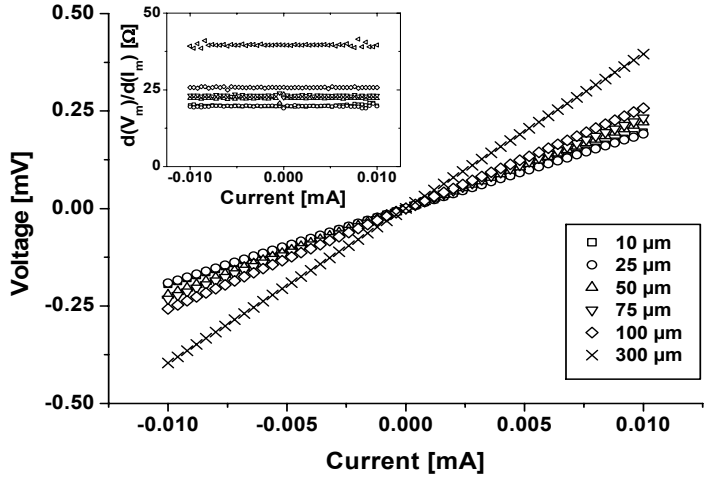
2.4 Results

2.4.1 'Design A'

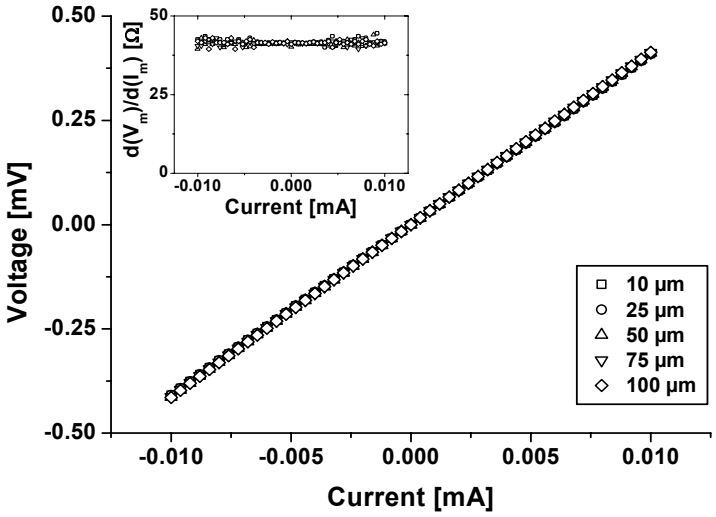
All devices are electrically characterized using the four-point method as described in section 2.2.2. The current I_{12} is forced between terminals 1 and 2 by application of a voltage, and here referred to as the 'measured current' I_m. The voltage, measured on terminal 3 and 4, V_{34}, is here referred to as the 'measured voltage' V_m. In this chapter, $V_m(I_m)$-characteristics are referred to as '*IV*-characteristics'.

For a 7 nm ALD TiN layer, *IV*-characteristics are measured from van der Pauw and Greek Cross structures having probe-to-probe distances of 10-300 μm (vdP) or central squares of 10×10 to 100×100 μm^2 (GC). All devices are measured over all 4 orientations. For vdP devices, the spread between 4 orientations ranges from 14 % to < 0.1 % for 10×10 to 300×300 μm^2 devices. For GCs, this is < 0.1 % for all devices.

The *IV*-characteristics for one of the four orientations are shown for vdPs (Figure 2.14a) and GCs (Figure 2.14b). For both sets of devices, linear *IV*-behaviour is observed. This is confirmed by plotting $d(V_m)/d(I_m)$, which is a constant function of I_m (see insets in Figure 2.14). For van der Pauw structures, a relatively large spread (11 %) in the *IV*-characteristics is observed for different device dimensions. For Greek Crosses this is not the case.



(a)



(b)

Figure 2.14: Measured V_m versus I_m-curves for van der Pauw (a) and Greek Cross (b) test structures ('Design A') for 7 nm ALD TiN for one of the four measurement orientations. The inset shows the corresponding $d(V_m)/d(I_m)$ versus I_m plots. Dimensions in the legends refer to the probe-to-probe distance (A, van der Pauw) and W value of the Greek Cross. The extra noise in the inset in $d(V_m)/d(I_m)$ for large I_m-values is due to a change in the measurement range of the measurement apparatus during the measurement.

From (solely) the slope of both sets of *IV*-curves, the ('measured') resistance ($R_m = V_m/I_m$) is calculated and averaged over the 4 orientations. The results are shown in Figure 2.15a. In Figure 2.15b, R_m-values are shown for a 4 nm ALD TiN layer. From Figure 2.15 it is observed that resistances extracted from van der Pauw structures (except for the 300 μm device) are significantly lower than those extracted from Greek Crosses. A slight increase in R_m is observed for larger devices. The reduced measured resistance may be related to the finite contact area (~2.5×0.1 μm^2) of the electrodes (i.e. not point-like contacts) in the van der Pauw structures [5, 10, 11].

Furthermore, for smaller devices the edge of the ALD layer is situated further away from the electrodes, thereby violating one of van der Pauw's boundary conditions, i.e. that the contacts should be at the circumference of the sample [5]. This is supported by measurements on the 300×300 μm^2 van der Pauw device in which the electrodes are close to the ALD layer edge: they yield virtually the same values for R_m as extracted from Greek Crosses.

2.4.1.1 Extracted sheet resistance

For Greek Cross devices of different dimensions, the sheet resistance (R_{sh}) can be calculated from R_m using a correction factor of π/ln(2) [7] and the results are shown in Figure 2.17. R_{sh} values of 186 and 720 Ω/□ are extracted for a 7 and 4 nm ALD TiN layer respectively.

For vdP structures, the standard correction factor of π/ln(2) cannot be used as the contacts are not at the circumference of the ALD TiN layer. The correction factors are obtained using the mathematical technique described in [78] and verified using a finite element analysis method.

In the analytical method, eq. (2.6) (see section 2.2.2) is solved using a conformal mapping technique and parameterised for standard square geometry as a function of the electrode position. Using Fig 4 in [81], the correction factors for vdP structures are extracted and shown in Table 2.1.

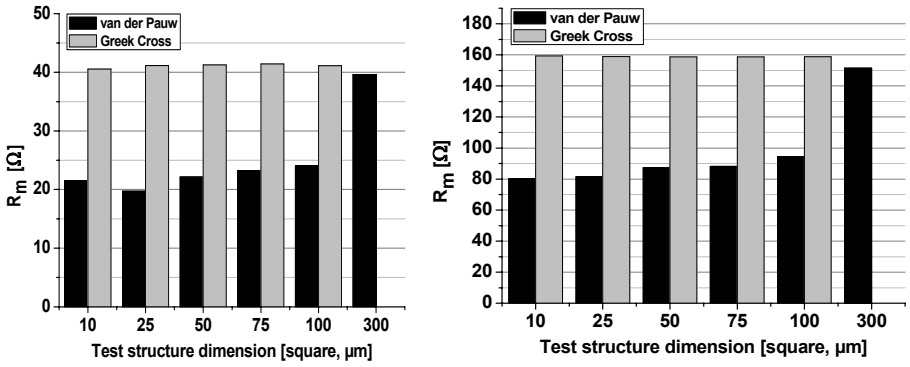


Figure 2.15: Extracted resistances (V_m/I_m) from van der Pauw and Greek Cross structures ('process A') for 7 nm (a) and 4 nm (b) ALD TiN layers. Resistances are an average of the 4 measured orientations.

These correction factors are verified by Finite Element (FE) simulations. The current and potential distributions are simulated for all vdP devices using MEDICI software [75, 82]. In Figure 2.16 the simulated potential distribution for a 10×10 µm^2 vdP device is shown. The contacts are situated at the corners of an imaginary square at a distance of 10 µm that is centered

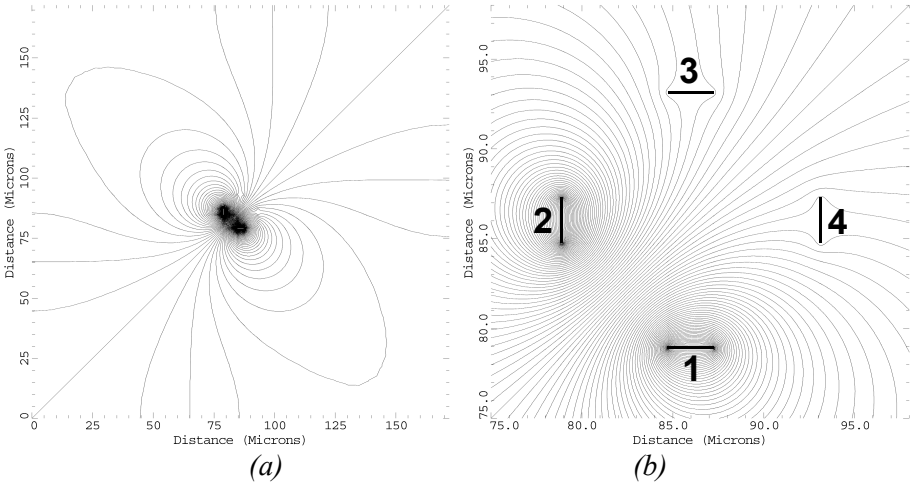


Figure 2.16: Simulated potential distribution for a 10×10 µm van der Pauw device with A = 10 µm, D = 172 µm and y=79 µm (see Figure 2.8a). Lines are equipotential lines. Whole device (a) and close up (b). Simulation obtained from [82].

with respect to the ALD film. The ALD film is patterned as a square with D=172 (see Figure 2.8a). A current (I) is forced between electrodes 1 & 2, while the voltages on electrodes 3 & 4 are determined (Figure 2.16b). From the voltage between electrode 3 and 4 (V_{34}), the current I, and a reference simulation on a device with the contacts at the circumference of the sample, the correction factor (C_f) is extracted. The simulated correction factors for all vdPs are shown in Table 2.1. It is observed that the correction factors extracted with the mathematical technique are in agreement with correction factors obtained using the finite element simulations. This shows that the mathematic technique can be used to obtain C_f in favour of the (time intensive) simulations.

Using the correction factors the sheet resistance values are calculated for van der Pauw structures of various dimensions and shown for 4 & 7 nm ALD TiN films in Figure 2.17 . It is observed the sheet resistance extracted from vdP and GC structures yield virtually the same values. The spread in the extracted sheet resistance for the 4 nm TiN is higher than for the 7 nm, this is most likely related to non uniformity (in thickness or resistivity) of the ALD TiN resistivity as these vdP devices are measured at different positions across the wafer (ρ varies over the position as will be shown in section 2.4.4).

It is concluded that both vdP and GC structures can be used to extract the sheet resistance and yield the same values for the sheet resistance for each layer thickness for a 7 and 4 nm ALD TiN layer.

A	***D***	***y***	**C_f analytical**	**C_f simulated**
µm	µm	µm		
10	172	79	**9.0**	**9.05**
25	356.5	161	**8.9**	**8.89**
50	356.5	143	**8.2**	**8.29**
75	500	197	**8.1**	**8.20**
100	500	179	**7.6**	**7.66**
300	530	53	**4.8**	**4.76**

Table 2.1: Correction factors for various van der Pauw devices obtained from an analytical [81] (a) or FE simulation method [75, 82] (b). Device parameters A, D & y are illustrated in Figure 2.8.

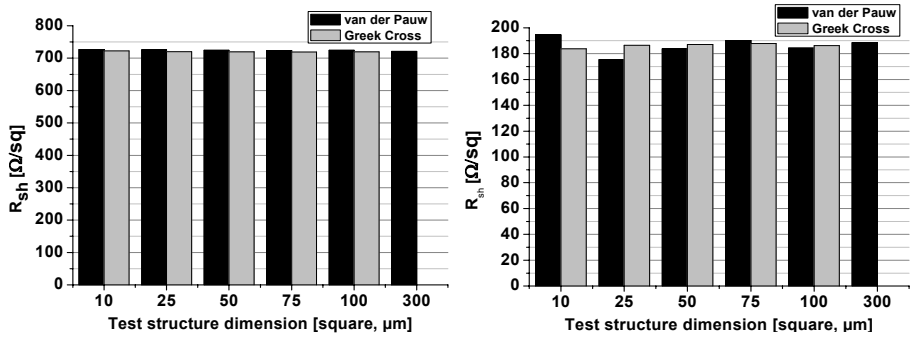


Figure 2.17: Sheet resistances values as a function of test structure dimension for 4 (a) & 7 nm (b) ALD TiN films, extracted from vdP and GC structures. For vdP data the correction factors in Table 2.1 are used.

2.4.2 'Design B'

For a 7 nm ALD TiN layer, *IV*-characteristics are measured from Greek Cross structures having *W* values of 8 and 50 µm. All devices are measured over all 4 orientations. The spread between 4 orientations is < 0.1 % for both devices.

The *IV*-characteristics of the first orientation are shown in Figure 2.18. For both devices, linear *IV*-behaviour is observed. This is confirmed by plotting $d(V_m)/d(I_m)$, which is a constant function of I_m (see inset Figure 2.19).

The measured resistance ($d(V_m)/d(I_m)$) is extracted and averaged over all 4 orientations. Using the standard correction factor of $\pi/\ln(2)$, sheet resistance values of 205 Ω/□ and 203 Ω/□ are found for the 50 µm and 8 µm devices, respectively. These values are within 10 % of the average R_{sh} value (~186 Ω/□) found for GCs with 7 nm TiN of 'design A'. It is concluded that GCs, fabricated in 'design A' and 'design B', yield almost identical R_m values for a 7 nm ALD TiN layer.

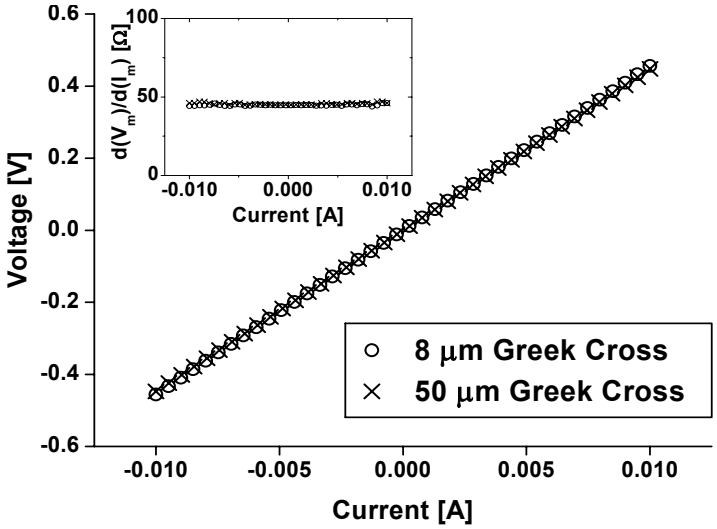


Figure 2.18: Measured V_m versus I_m curves for Greek Cross structures ('design B') for one of the four orientations, for a 7 nm ALD TiN. The inset shows the corresponding dV_m/dI_m versus I_m. Dimensions refer to W-value of the Greek Cross.

2.4.3 Resistivity

The resistivity (ρ) is, according to equation (2.9), calculated from R_{sh} and the layer thickness and extracted for 'design A' and 'design B'. These results are shown in Figure 2.19 together with results of a TiN thin film (ALD from $TiCl_4$ and NH_3 at 400 ºC) measured by Langereis and co-workers [12].

It is shown that, for thick layers (> 12 nm), approximately the same resistivity is observed for the results from literature and our layers. This shows the bulk resistivity of both films is approximately equal. For thinner films, the extracted resistivity is a function of the layer thickness.

The extracted resistivity values are higher for thinner films than the literature values, but realistic [53, 57, 83]. For both sets of data, the same trend of increasing resistivity with decreasing layer thicknesses is observed. For extremely thin films the mean free path (L_{mfp}) of electrons becomes larger than the film thickness, resulting in increased scattering at the thin film interface and hence a higher resistivity [84, 85].

The higher ρ-values for thin films for our measurements with respect to literature results can be due to differences in the metrology. The literature ρ-values are extracted from modelling of optical data using Drude-Lorenz parameterization obtained from *in situ* SE measurements. The extraction of ρ includes correction for its temperature dependence: it is extracted at ~400 °C and calculated back to room temperature values using the temperature coefficient of resistance (TCR). The same TCR value is used for all TiN layer thicknesses [13]. As the TCR is lower for thinner films (see Figure 2.22, section 2.4.5), this can contribute to lower ρ-values in literature.

Furthermore, in SE method, the extracted resistivity is solely based on modelling of optical data in terms of the mean free path and electron density (D_{el}) [86]. With the interpretation of this data care has to be taken with respect to grain boundaries in the thin film. Thin films have smaller grains and hence more grain boundaries per unit volume. In electrical measurements, a higher grain boundary density has a direct influence on the conducted current: more scattering on grain boundaries results in a higher resistivity.

For the SE method, the effect of grain boundaries affects the mean free path of electrons *inside* grains which is modelled, not the barrier *between* grains.

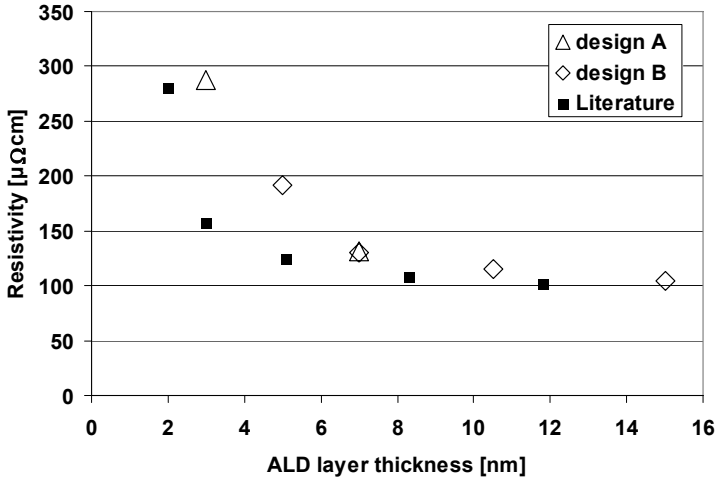


Figure 2.19: Resistivity versus layer thickness for ALD TiN films extracted from measurements on 'design A' & 'design B'. Literature values are reprinted from [44].

And this barrier, which is not considered by SE, is of prime importance for carrier dynamics under applied bias.

This indicates that the ρ-values extracted from electrical measurements are more thrustworthy than those obtained from the optical method.

It is concluded that all devices from 'design A' and 'design B' yield realistic values for the resistivity and can be used successfully for the determination of the resistivity of thin ALD TiN films with thicknesses in the range of 4-15 nm.

2.4.4 Uniformity of the ALD TiN process

In order to characterize the sheet resistance uniformity of the ALD TiN layer over a 100 mm wafer, a layer of 10.5 nm of ALD TiN was measured using GC structures ('design B') at various positions on the wafer. In Figure 2.20 a wafer map of the sheet resistance is shown. A variation in sheet resistance as function of the position on the wafer is observed. The average sheet resistance is 103 Ω/□ with a standard deviation of 9 Ω/□. The non-uniformity in sheet resistance of the ALD TiN layer may be related to the gas flows in system with respect to the wafer and/or a non-homogeneous temperature distribution in the ALD reactor chamber (the wafer is not rotating during deposition) [61].

The data shows that there is a variation of ca. 9 % in thickness or resistivity of the ALD TiN layer over a 100 mm wafer.

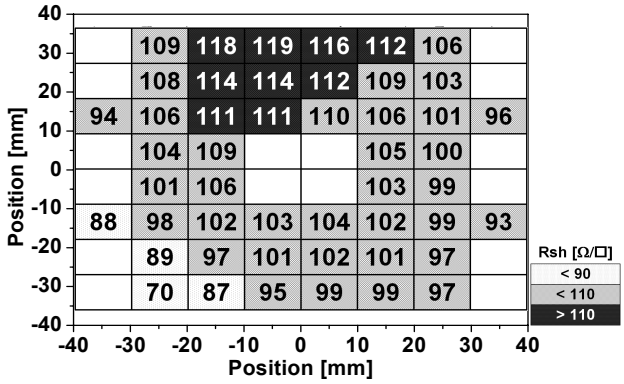


Figure 2.20: Wafer map of the sheet resistance for a 100 mm wafer with a 10.5 nm ALD TiN layer. (0,0) is the centre of the wafer.

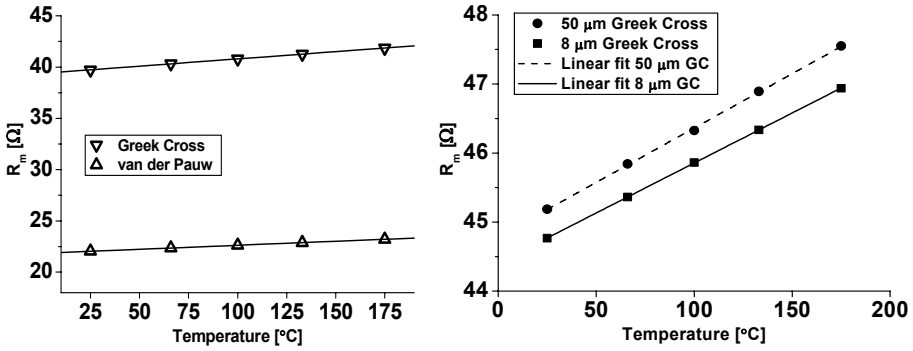
2.4.5 Temperature dependence of the resistivity

2.4.5.1 Low temperature range: up to 175 ºC

For a 7 nm ALD TiN layer, the resistance is measured at several temperatures in the range of 25-175 ºC. The results for a 75 µm vdP and GC device ('design A') and for 8 and 50 µm GC devices ('design B') are shown in Figure 2.21. A linear relation between resistance and temperature is observed for all devices.

The TCR is extracted, according to equation (2.13), from the fitted linear slope and the (extrapolated) resistance at 0 ºC. TCR values of 3.6×10^{-4} /ºC are extracted for the vdP and GC devices of 'design A' and values of 3.3×10^{-4} /ºC and 3.5×10^{-4} /ºC for the 8 µm and 50 µm GC devices of 'design B'.

These results are shown in Figure 2.22 together with the TCR values of other TiN thin films with thicknesses in the range of 4-15 nm layers. The data is shown as a function of the corresponding resistivity as ρ is a function of the layer thickness, but also of other factors such as the TiN stiochiometry



(a) *(b)*

Figure 2.21: Measured resistance versus temperature of 75 µm van der Pauw and 75 µm Greek Cross devices ('design A', (a)) and 8 and 50 µm Greek Cross devices ('design B', (b)) for a 7 nm ALD TiN layer. Lines are linear fits through the data. TCR values of 3.6×10^{-4} /ºC ((a), both vdP & GC) and 3.3×10^{-4} /ºC and 3.5×10^{-4} /ºC are extracted for 8 and 50 µm GCs (b), respectively.

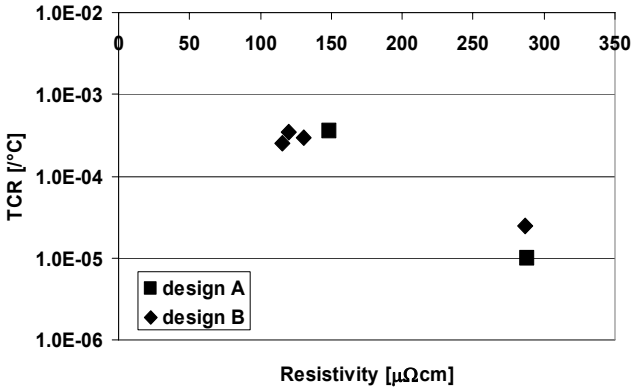


Figure 2.22: TCR versus resistivity for various TiN thin films (4-15 nm) measured using GC structures of 'design A' and 'design B'.

or contamination (Cl, O, H) [44]. ALD TiN layers with a resistivity of ~1×10^{-4} μΩcm have a TCR in the mid 10^{-4} /ºC range. For layers with a resistivity of ~3×10^{-4} Ωcm, a TCR in the low 10^{-5} /ºC range is observed.

It is concluded that thinner ALD TiN layers have a higher resistivity and lower TCR values.

2.4.5.2 High temperature range: up to 700 ºC

2.4.5.3 Substrate: silicon with 100 nm SiRN

Samples were measured up to 700 °C in a special high temperature setup at NXP research facilities in Eindhoven. In the setup, a 2×2 cm sample with a GC of 'design A' (patterned TiN with passivation) or a blanket (unpatterned and unpassivated) ALD TiN film was measured. The sample was contacted with 4 fixed tungsten probes which were arranged at the corners of a 10×10 mm square. The sample was fixed with silver glue to an aluminium nitride (AlN) sample holder. The temperature was measured with a thermocouple in the AlN sample holder. During operation, the system is pumped down to a pressure 2×10^{-7} Torr. The resistance was measured by forcing a current of 0.1 mA via a Keithley 220 programmable current source (in combination with a Keithley 705 scanner for channel selection) while measuring the voltage using a Keithley 2000 multimeter. The measurement current was low enough to avoid self heating of the sample during the

measurement. The temperature versus the time and electrical measurements were controlled by a computer with Labview.

For a 7 nm ALD TiN layer, the resistance is measured with a GC structure ('design A') between 150-450ºC and shown in Figure 2.23. Between 150-200 ºC a linear relation between resistance and temperature is observed, while for temperatures above ~230 °C a strong decrease (factor 10) in resistance is shown. This decrease is almost reversal; the resistance at 150 ºC decreases from 36.3 Ω before to 30.6 Ω after sweeping to 450 ºC. Lowering of the resistance at 150 °C is most likely a result of the high temperature step itself (as will be shown shortly in Figure 2.25). The slope in the linear part of R(T) between 150-200 ºC is also different after sweeping to 450 ºC. Different TCR values of 2.5×10^{-4} /ºC (before reaching 450 ºC) and 6.0×10^{-4} /ºC (after reaching 450 ºC) are extracted.

During the measurements on the TiN layer, a dielectric layer (100 nm SiRN) separates the TiN layer from the silicon substrate. This is schematically shown in Figure 2.24a. At higher temperatures, we found the dielectric layer loses its insulating properties [8] and a leakage current through the silicon substrate is flowing parallel to the TiN layer. In other words: the resistance of the silicon wafer is measured parallel to the TiN resistance (Figure 2.24b).

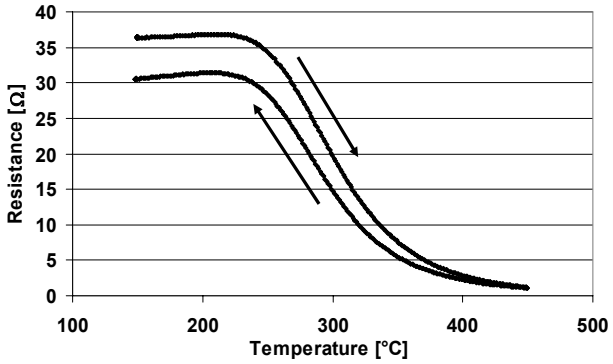


Figure 2.23: Resistance vs temperature for a 7 nm ALD TiN layer measured with a 25×25 μm GC structure ('design A'). The temperature is ramped from 150 ºC up to 450 ºC and down with +/- 5 ºC / min. The TCR can be extracted from the linear regime between 150-200 ºC.

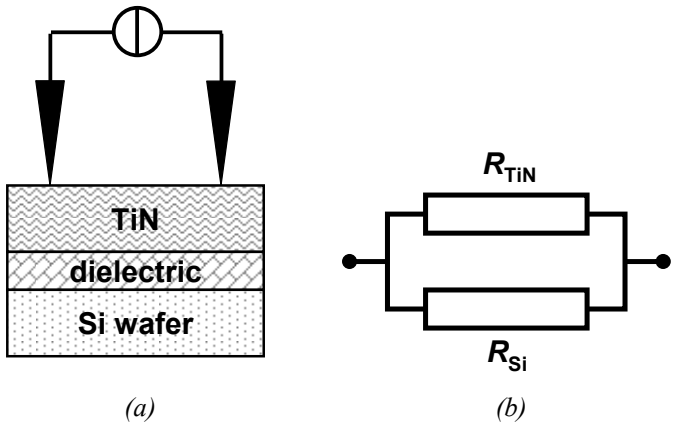


Figure 2.24: Schematic cross-section of the van der Pauw structure ('design A') with measured (I_m) and leakage (I_{leak}) current (a) and corresponding resistance model (b).

The silicon resistance depends on its charge carrier concentration. The intrinsic charge carrier concentration n_i in silicon is a strong function of the temperature and increases by 5 orders of magnitude between 0 and 200 ºC [87]. At low temperatures, the resistivity of doped silicon is high. It is dominated by the majority charge carrier concentration [88]. Above a certain critical temperature (T_c), the intrinsic carrier concentration exceeds the majority carrier concentration, leading to an exponential drop in the silicon resistance [88, 89]. This is confirmed by experiments on the silicon sheet resistance at elevated temperatures using GC structures by Corvasce *et al.* [90].

2.4.5.4 Substrate: quartz with 100 nm SiRN

In order to exclude the influence of the silicon substrate on the measured TiN resistance, an additional experiment was carried out. A 7 nm ALD TiN layer is deposited on a quartz substrate with 100 nm SiRN. The layer was unpatterned and without the Al_2O_3/SiO_2 passivation used in 'design A' and 'design B'. Electrical measurements up to 700 ºC on this film were carried out in an experiment in which the temperature is ramped up repetitively from 150 ºC to an increasing maximum temperature (T_{max}) and back to 150 ºC (see Figure 2.25). In Figure 2.26, the resistance versus the temperature is shown.

A decrease in resistance at 25 ºC from 37 Ω to 27 Ω is observed between the start and end of the experiment. Furthermore, linear $R(T)$ relations are observed up to 700 ºC for temperatures 100 ºC lower than T_{max}. It is shown that every time when the temperature exceeds the maximum (annealing) temperature of the previous sweep, the resistance decreases irreversibly. These results confirm that the decrease in measured resistance above ~230 ºC in Figure 2.23 is related to the presence of the silicon substrate and not a property of the TiN layer (nor the 100 nm SiRN layer).

Furthermore, these results indicate that the TCR of ALD TiN layers, determined at temperatures between 25-175 ºC on silicon substrates (coated with 100 nm SiRN) as shown in section 2.4.5.1, remains constant up to 600 °C, provided the sample has been heated up to 700 ºC.

From the linear parts in Figure 2.26, the TCR is extracted and shown in Figure 2.27 as function of the maximum anneal temperature (T_{max}). An increase in TCR from 1.0×10^{-4} /ºC for T_{max} = 200 ºC to 2.1×10^{-4} /ºC for T_{max} = 700 ºC is observed. These results show that the effect of the annealing step up to 700 ºC on the TCR of the ALD TiN film is practically speaking small, but needs to be taken into account for an accurate TCR measurement.

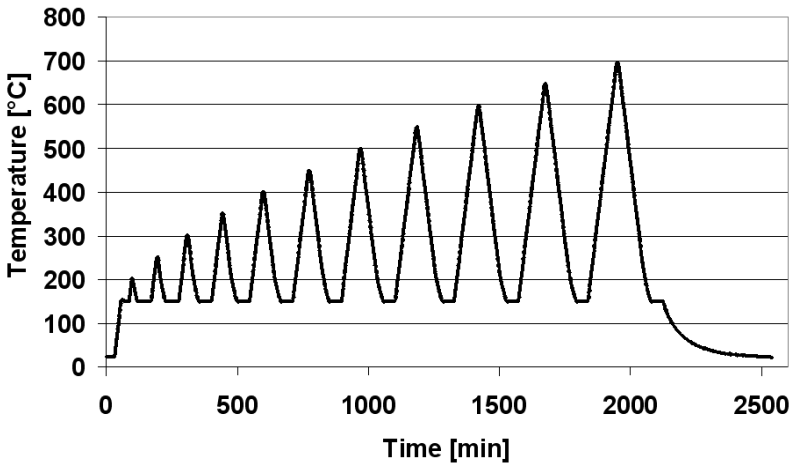


Figure 2.25: Temperature vs time for a 7 nm ALD TiN layer deposited on a quartz substrate (coated with 100 nm SiRN). The temperature is increased to 150 ºC and from this temperature ramped up to T_{max} and down to 150 ºC, with T_{max} increasing up to 700 ºC.

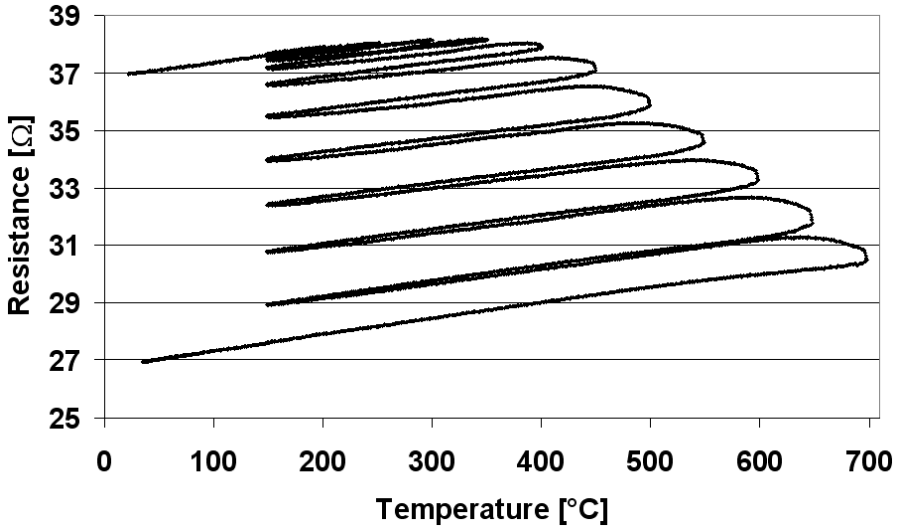


Figure 2.26: Resistance vs temperature for a 7 nm ALD TiN layer deposited on a quartz substrate (coated with 100 nm SiRN) The corresponding temperature vs time profile is shown in Figure 2.25.

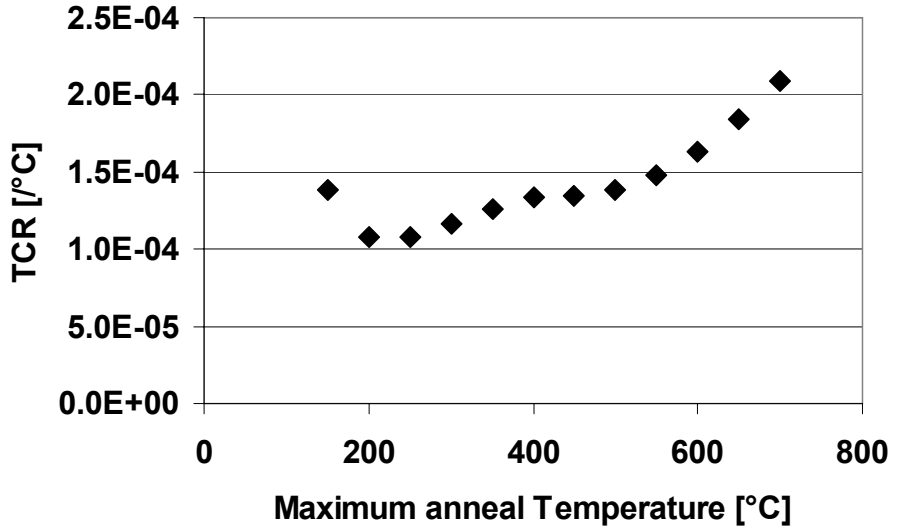


Figure 2.27: Temperature coefficient of resistance (TCR) vs maximum anneal temperature (T_{max}) for a 7 nm ALD TiN layer deposited on a quartz substrate with 100 nm SiRN.

2.5 Conclusions

In this chapter, the electrical properties of ALD TiN thin films are investigated using a four-point methodology. Special four-point probe test structures like vdPs and GC are presented to overcome problems in electrically contacting thin ALD TiN films. Test structures of two different designs were fabricated in two different process architectures. In 'design A', the ALD TiN film is deposited on a flat surface which is obtained by incorporating a CMP step in the fabrication process. In 'design B' the ALD TiN layer is deposited on a surface having topography, but is fabricated without the cumbersome CMP step. Using these test structures, the resistance is measured for ALD TiN layers with a thickness in the range of 4-15 nm. Test structures of 'design A and B', yield similar results. The thin film resistivity is extracted from the sheet resistance and layer thickness. It is shown that the resistivity increases with decreasing the layer thickness. Both test structures can be used successfully to characterize ultrathin ALD TiN films.

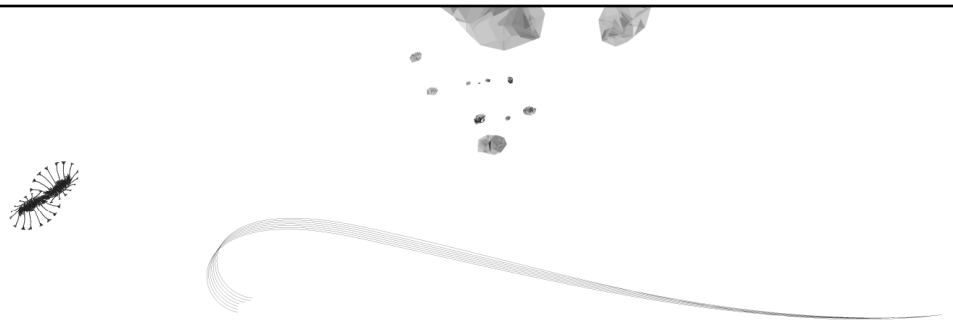
The TCR of ALD thin films is measured up to 175 ºC and shown to be correlated to the thin film resistivity. Thinner ALD TiN layers have a higher resistivity and lower TCR values.

Measurements at temperatures up to 700 ºC in vacuum (annealing) showed that every time when the temperature exceeds the maximum annealing temperature, the resistance at 25 ºC and 150 ºC irreversibly decreases together with a small change in the TCR (in practice).

Furthermore, for ALD TiN films on silicon substrates, coated with 100 nm SiRN (for insulation), a strong and reversal decrease in measured resistance for temperatures above ~200 ºC is observed. It is shown that, using quartz substrates with 100 nm SiRN, this is due to a leakage path through the silicon substrate parallel to the TiN layer as result of the SiRN layer losing its insulating properties. Furthermore, it is shown that the TCR, extracted from TiN films on silicon substrates with 100 nm SiRN up to 175 ºC, remains constant for temperatures up to 600 ºC, provided the sample has been heated up once to 700 ºC.

3

The oxidation of ALD TiN films



3.1 Outline

In this work ALD TiN films are used as heating element in SMAs, aiming to reach temperatures of 300-500 ºC. During operation of the SMA at elevated temperatures and in an oxygen containing ambient, the ALD TiN layer should not oxidize. It is of prime importance to know the oxidation behaviour of the ALD TiN layer.

TiN is known for its high thermodynamic stability and high corrosion resistance [91, 92]. However, the properties of TiN are strongly influenced by the film stoichiometry, crystallinity, morphology and hence the deposition method [83, 93]. Sputtered TiN layers with 1:1 stoichiometry are known to oxidize significantly in dry ambient (O_2) above 500 ºC [94, 95], non-stoichiometric TiN layers (Ti_1N_{1-x}) even at room temperature [96].

During fabrication of SMAs, the ALD TiN thin film in the SMA is likely to be exposed to low-temperature oxidizing ambients; for instance primers, (pre-)bakes, cleaning and dielectric deposition such as the fabrication of an SiO_2 layer by chemical vapour deposition (CVD) from SiH_4 and N_2O [63]. Therefore, oxidation of ALD TiN at atmospheric conditions (dry (O_2) and wet (H_2O)), as well as in an inductively coupled Ar/N_2O plasma is investigated. The corresponding oxidation kinetics of ALD TiN are obtained.

Oxidation of TiN films can be avoided by the deposition of a blocking or passivation layer on the ALD TiN. In this chapter, the functionality of 25-50 nm thick passivation by layers of Si_3N_4, SiO_2 and Al_2O_3 is described.

3.2 Experimental

ALD TiN layers of 8 nm (400 cycles) were grown from $TiCl_4$ & NH_3 at 425 ºC in reactor 2 of the cluster system (see section 1.3.1) on standard *p*-type silicon wafers with 100 nm thermally grown (O_2 ambient) SiO_2. Before deposition, samples were cleaned in 100 % HNO_3 for 10 min followed by immersion in boiling 69 % HNO_3 for 10 min, and dipped in 1 % HF for 30 s. For structural analysis of TiN layers (see further in this paragraph: RBS and HRTEM analysis), silicon substrates without thermally

grown SiO_2 were used. After ALD of TiN, several samples were passivated by 50 nm ALD Al_2O_3, [61] and with 40 nm ICPECVD SiO_2 or 25 nm ICPECVD Si_3N_4 [63]. A number of TiN samples were passivated with a ('standard') 50 nm SiO_2 layer, deposited from SiH_4 and N_2O at 300 ºC in a Plasmalab80plus PECVD system by Oxford Instruments (i.e. PECVD SiO_2).

The samples were oxidized in a horizontal tube furnace in dry (4 sccm N_2, 1 sccm O_2) or wet (H_2O bubbler with N_2 at 30 ºC) ambient in the temperature range of 350-500 ºC. The plasma oxidation was carried out in an inductively coupled plasma (ICP) reactor at 300 W ICP-RF power, a pressure of 6×10^{-2} mbar, 200 sccm of Ar flow and 44 sccm of N_2O flow, and temperatures in the range of 25-300 ºC. The oxidation process was ex-situ (dry / wet oxidations) or *in situ* (plasma) monitored using a spectroscopic ellipsometer (SE) Woollam M2000DI operated over the wavelength range of 245 to 1688 nm (see section 3.3) [96]. Furthermore, both the thickness and composition of as-deposited (AD) and oxidized TiN layers were verified by Rutherford Backscattering Spectroscopy (RBS) in combination with elastic recoil detection (ERD). Partially oxidized samples were investigated using Energy Filtered High Resolution Transmission Electron Microscopy (EF-HRTEM).

3.3 Spectroscopic Ellipsometry

Spectroscopic Ellipsometry (SE) is a very sensitive non-destructive surface and thin film optical measurement technique that uses polarized light. SE measures the polarization state of the light beam reflected from a sample. The polarization state of the light is measured in terms of ellipsometry parameters psi (Ψ) and delta (Δ), both as a function of the wavelength (λ) [41, 97]. A model of the sample containing optical constants of the layer stack is used to generate Ψ- and Δ-data which is fitted to the measured data by using the layer thicknesses as fitting parameters. The difference between the fitted (model) and the measured Ψ and Δ-data is quantified in terms of the Mean Square Error (MSE). The MSE is a dimensionless quantity. In this work, the optical stack is modelled using a

combination of standard ('Woollam') models with optical constants of all the layers used. The angle offset of the optical beam, which is slightly different for each ex-situ measurement, is taken into account as well. For modelling dry and wet oxidation, a stack consisting of TiO_2/TiN/SiO_2/Si(substrate) is used with the TiO_2 and TiN thicknesses and the angle offset as fitting parameters.

3.4 Results

3.4.1 Oxidation

3.4.1.1 Dry and wet oxidation of ALD TiN

In Figure 3.1 the TiN and TiO_2 thicknesses versus oxidation time (t) are shown for wet oxidation at 400 ºC, together with the Mean Square Error (MSE) of the fitted optical model. Each point corresponds to a single experiment (i.e. loading of the sample in the furnace, oxidation, unloading, followed by ex-situ SE) and the time to the total (cumulative) oxidation time. At t = 0 min, a TiN thickness of 8 nm is observed and a TiO_2 thickness of 3.5 nm. This initial TiO_2 layer is the native oxide formed by oxidation in air

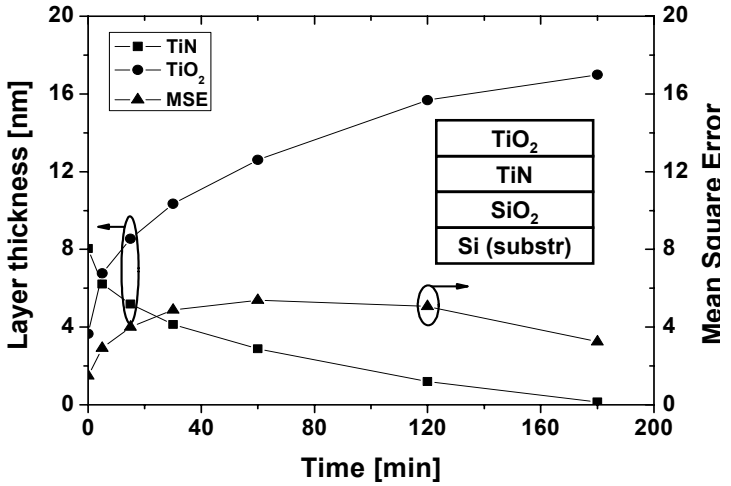


Figure 3.1: TiN and TiO_2 thickness vs time together with the Mean Square Error (MSE) of the fit of the optical model for wet oxidation at 400 ºC. The inset shows the optical model used.

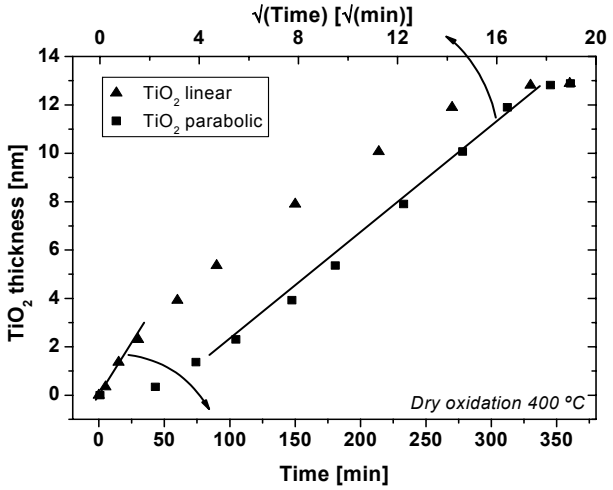
at room temperature after finishing the deposition of the TiN layer. During oxidation of the TiN layer, a decrease in TiN thickness together with an increase in TiO_2 thickness is observed. The 8 nm TiN is converted to approximately 12 nm TiO_2 in addition to the initial 3.5 nm TiO_2 after complete oxidation. The ratio of TiN/TiO_2 thicknesses (i.e. 8 nm TiN → 12 nm TiO_2) is in agreement with literature about the oxidation of stoichiometric sputtered TiN layers [94]. The MSE increases during the first part of the oxidation and decreases for the last part. This might be the result of the limited applicability of the standard layer-by-layer optical models for TiN and TiO_2 used in this work and the properties of the TiN and TiO_2 layers (i.e. zero roughness of the layers) to model the oxidation process [62].

In Figure 3.2, the TiO_2 thicknesses versus the oxidation time (t) are shown for the dry and wet oxidation at 400 ºC at a linear (t) and parabolic ($\sqrt{t}$) time scale. Two regimes are distinguished: in the first (initial) regime, the TiO_2 thickness increases rapidly, in the 2nd regime it follows a parabolic relation. Given the short oxidation times for the initial regime, the uncertainty of this data is relatively high, since for example loading of the sample into the furnace might contribute to additional TiO_2 growth. The existence of two regimes indicates that the oxidation mechanism follows the classic Deal-Grove oxidation model [98]. For the initial regime, the formation of the first 3-6 nm of TiO_2 is, most likely, limited by the reaction kinetics. For the parabolic regime, the oxidation is limited by the diffusion of oxidizing species through the oxide layer.

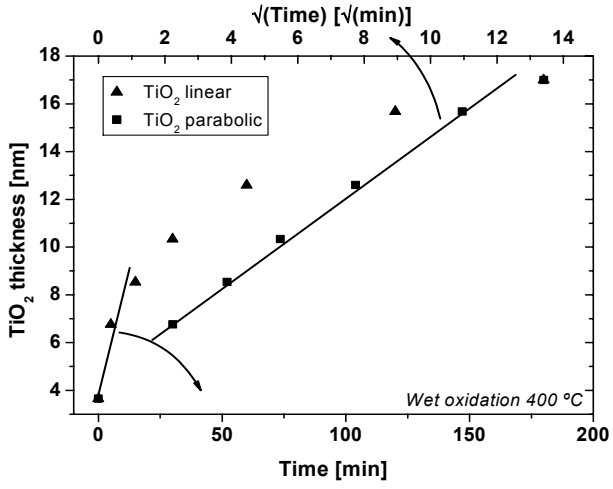
The oxidation rate of TiN is extracted from slope of the linear parts of the oxidation curves at several temperatures, these rates are used to construct Arrhenius plots as shown in Figure 3.3. The error bars in the data are the (1σ) uncertainties in the extracted oxidation rates. The activation energies of the dry and wet oxidations are extracted from the slope of a linear (σ-weighted) fit in the Arrhenius plots, for both the initial (Figure 3.3a) and parabolic (Figure 3.3b) regimes. For the initial regime, values of 1.1 ± 0.1 eV and 0.9 ± 0.2 eV are found for dry and wet oxidations respectively, and 2.0 ± 0.1 eV (dry) and 1.3 ± 0.1 eV (wet) for the parabolic regime.

The activation energies for the parabolic regime are in agreement (within 13 %) to those obtained for sputtered TiN [94], the initial oxidation regime is not reported in the literature to our best knowledge.

The activation energy of ~1 eV for the initial regime shows that ultrathin ALD TiN films are sensitive for oxidation and need to be protected during processing. For example, when an 8 nm TiN layer is oxidized down



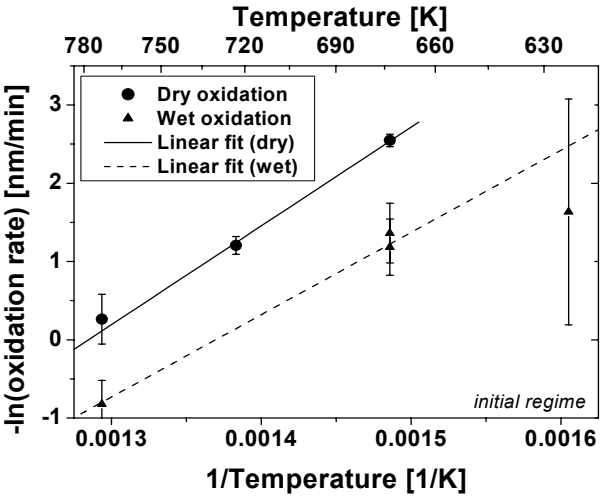
(a)



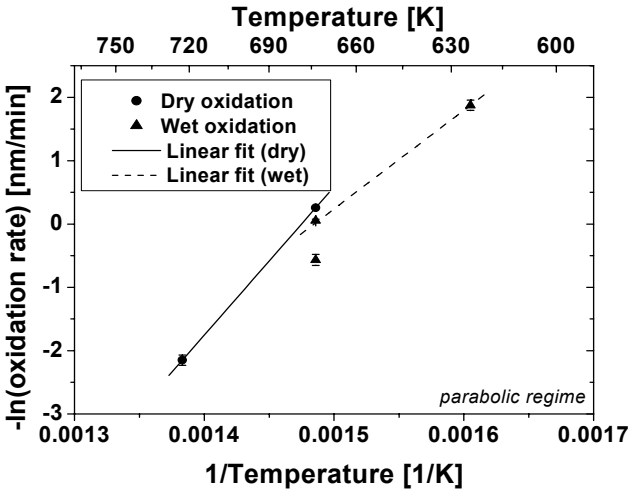
(b)

Figure 3.2: TiO_2 thickness vs time for dry (a) and wet (b) oxidation at 400 ºC.

to 7 nm (takes ~5 or ~3 min in dry / wet ambient at 400 ºC), this results in a change in TiN resistivity (see Figure 2.19) and hence a change in TCR (see Figure 2.22). This is undesired as it could lead to misinterpretation of the temperature in SMAs.



(a)



(b)

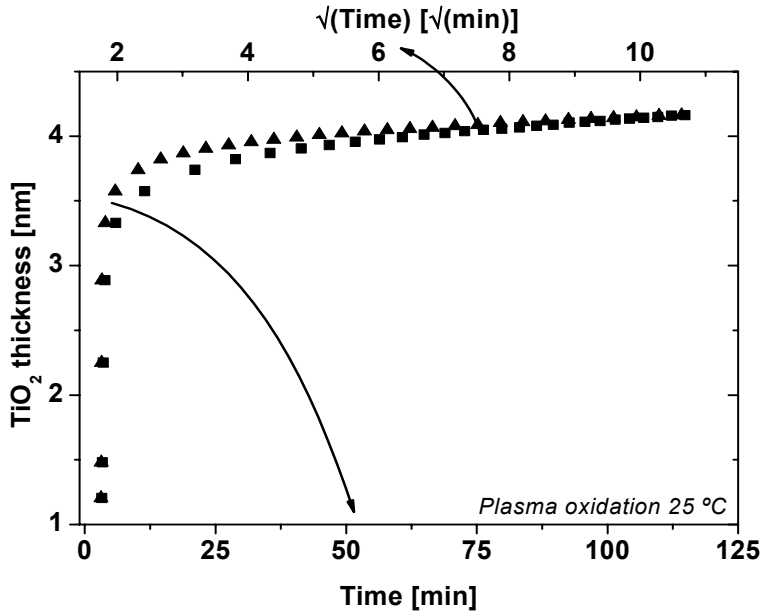
Figure 3.3: Arrhenius plots for dry and wet oxidation of ALD TiN films for initial (a) and parabolic (b) regimes. Lines are error weighted linear fits through the data.

Thus, it is required that ultrathin ALD TiN layers, applied as heater material in SMA-type hotplates, need to be protected with a passivation or 'blocking' layer to avoid any oxidation during processing and operation of the device at elevated temperatures. The influence and functionality of different materials that can be used as passivation for TiN thin films are described in section 3.4.3.

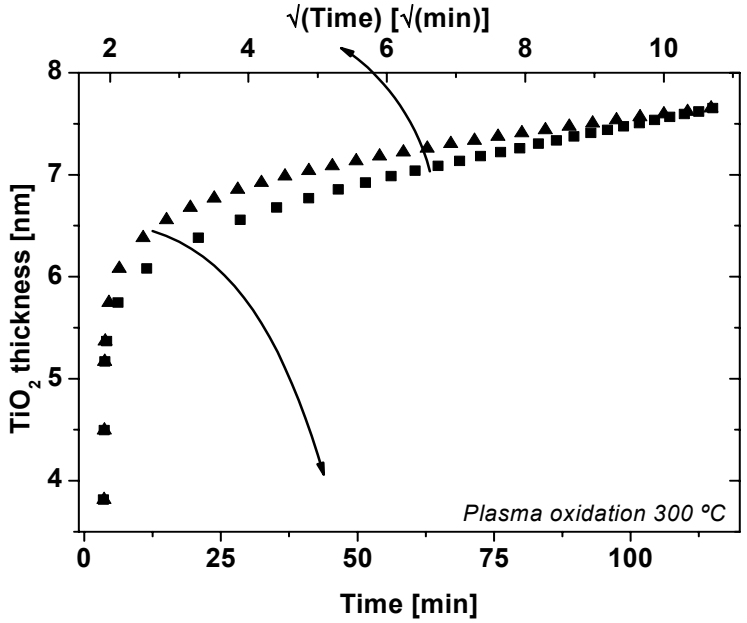
3.4.1.2 Plasma oxidation of ALD TiN

In Figure 3.4, the TiO_2 thickness versus time is shown for plasma oxidation at 25 ºC and 300 ºC. Clearly two oxidation regimes can be distinguished. The first regime (the first few minutes only) is linear with a slope of ~1.8 nm/min for both temperatures. The second regime also exhibits a close-to-linear behaviour for the measured oxidation times up to 125 min. A linear fit clearly two different slopes for the 2nd regime, namely ~2×10^{-3} nm/min for 25 ºC and 8×10^{-3} nm/min for 300 ºC. The existence of two regimes indicates two different oxidation mechanisms. In the very narrow first regime, the oxidation rate can be limited by temperature-independent processes such as e.g. electron tunnelling through the growing oxide [99, 100] or oxidation by excited oxygen species (radicals) present in the N_2O-Ar plasma [101, 102].

The results show that, if a PECVD SiO_2 layer is planned to be deposited on top of an ultrathin ALD TiN layer, the TiN layer will be oxidized significantly (~2 nm) during the first minute of the deposition. In case PECVD SiO_2 is used as a passivation layer for ALD TiN, another layer, for instance ALD Al_2O_3 should be applied first without vacuum break. This is necessary to avoid oxidation of the ALD TiN layer by the plasma during the SiO_2 deposition (see section 3.4.3).



(a)



(b)

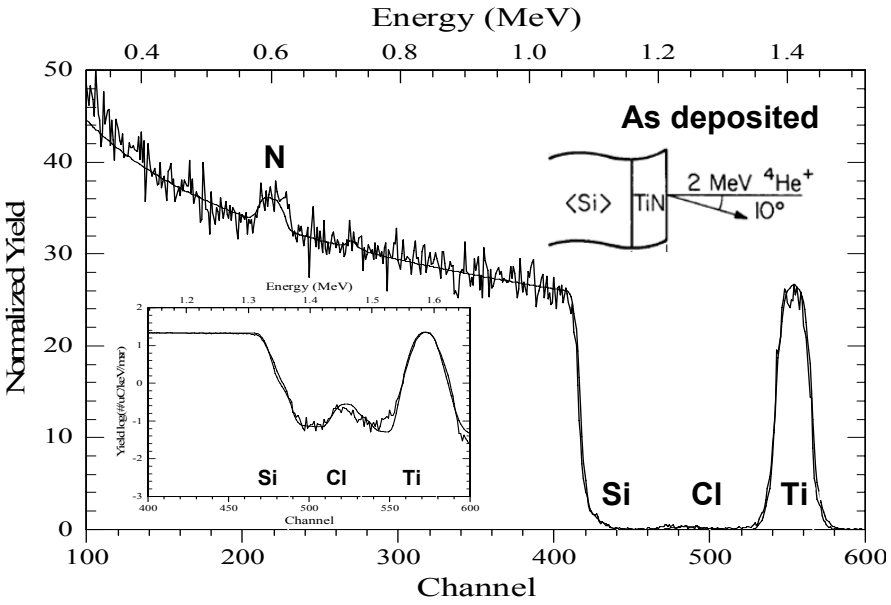
Figure 3.4: TiO_2 thickness vs time for plasma oxidation of ALD TiN at 25 °C (a) and 300 °C (b), obtained from in situ SE monitoring.

3.4.2 Material characterization

3.4.2.1 RBS

The elemental composition of as-deposited and fully oxidized TiN samples was examined by means of Rutherford Back Scattering (RBS). RBS was done using a beam of 2 MeV He^+ in combination with a detector positioned at 10º with respect to the incoming beam, and a second detector for elastic recoil detection (ERD) of hydrogen. A layer of ~20 nm TiN was deposited on a silicon substrate without thermally grown SiO_2, broken into two parts, and half of the sample was fully oxidized in wet ambient at 500 ºC for 45 min. The RBS spectra of both as-deposited and fully oxidized samples are shown in Figure 3.5. For the as-deposited sample, the best model fit through the data yields an areal density of 10×10^{15} at/cm^2 TiO_2 on top of $Ti_1N_1Cl_{0.02}H_{0.05}$, having 190×10^{15} at/cm^2. For the oxidized sample, an areal density of 300×10^{15} at/cm^2 of $Ti_1O_2Cl_{0.01}H_{0.035}$ is found. Given the accuracy of the analysis method, it is concluded the TiN layer is stoichiometric within 10 %. The fraction of Cl is most likely the result of a partly decomposed precursor ($TiCl_4$), the hydrogen is most likely bound as OH-groups on the top surface of the TiO_2 layer [103].

The areal densities of can be converted to layer thicknesses by assuming bulk densities of 10.16×10^{22} at/cm^3 for TiN and 9.63×10^{22} at/cm^3 for TiO_2, respectively [77]. This yields layer thicknesses of 1.6 nm for TiO_2 and 18.7 nm for TiN for the as-deposited sample, and 31.2 nm for the oxidized sample. The ratio of TiN/TiO_2 thicknesses before and after oxidation (18.7 nm TiN → 31.2 nm TiO_2), extracted from RBS measurements, is in agreement with the thickness ratio, extracted from SE measurements, of an 8 nm ALD TiN layer (as discussed in section 3.4.1.1).



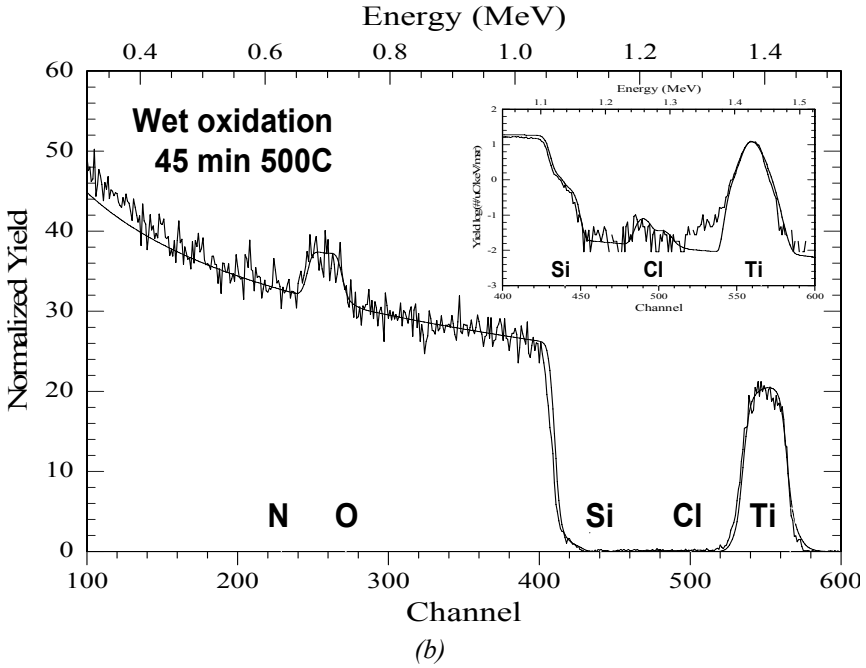


Figure 3.5: RBS spectra of as deposited (a) and fully oxidized TiN layers (b). The inset shows a close-up of the signal in the vicinity of the Si-Cl-Ti peaks on a logarithmic scale.

3.4.2.2 HRTEM

A HRTEM cross-section of a partly oxidized sample (25 nm of TiN on Si followed by a wet oxidation at 400 ºC for 2 hours) is shown in Figure 3.6. The TiN grains of ca. 20 nm are oriented perpendicular to the surface of the silicon substrate, covered by an non-uniform layer of polycrystalline TiO_2. Furthermore, a very thin layer of SiO_2 is observed between the Si substrate and the TiN thin film. Since the native oxide on the silicon substrate was etched in 1 % HF before the TiN deposition, this SiO_2 layer was formed during the ALD process of TiN, most likely during the heating up phase before the actual TiN deposition. This result shows that the TiO_2 and TiN layers are non-homogeneous in thickness.

3.4.2.3 EFTEM

The elemental composition of the partially oxidized sample was measured using EFTEM and is shown in Figure 3.7a. The elemental maps in Figure 3.7a are quantified and integrated over the selected square areas, resulting in the depth profiles shown in Figure 3.7b. Allthough both signals show a little difference (ca.30 %), the reduced titanium (Ti) signal close to the surface is in accordance with the TiO_2/TiN layer composition. The same applies to the higher oxygen signal near the surface and the higher nitrogen

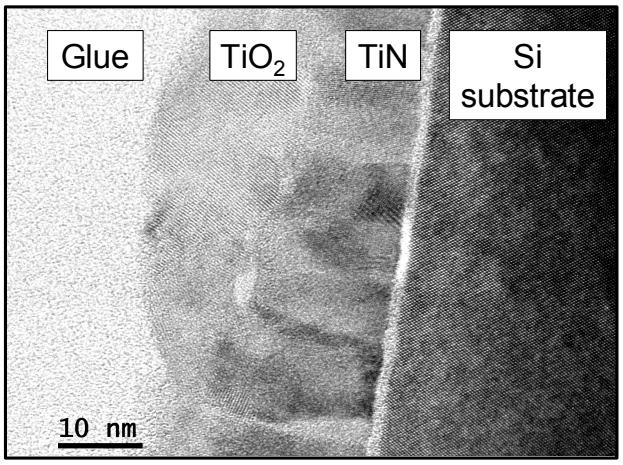


Figure 3.6: HRTEM cross-section of a partly oxidized TiN sample; 25 nm TiN on a silicon substrate after wet oxidation at 400 ºC for 2 hours.

signal near the substrate. However, a relatively large oxygen signal near the substrate is observed. Probably this is a result of oxygen diffusion into the TiN via the grain boundaries [104]. As the sample for EFTEM is relatively thick (i.e. the thickness/depth in the direction of the electron beam, ~50-100 nm), multiple grain boundaries at various positions within the layer contribute to the TEM image, leading to an averaged-in-space oxygen map. The same applies to the relatively large nitrogen signal near the wafer surface.

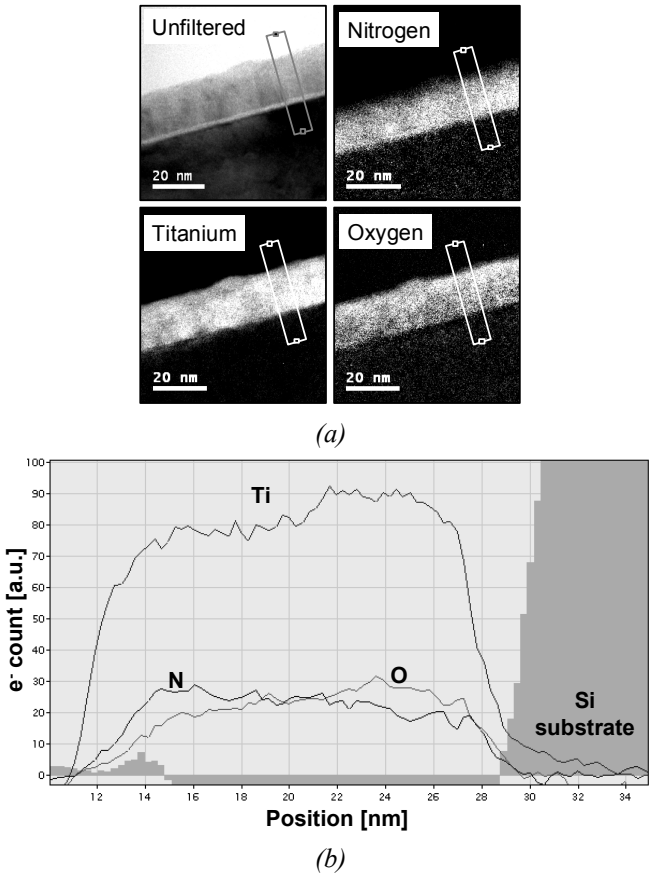


Figure 3.7: Elemental mappings (a) using energy filtered TEM (EFTEM) of a partially oxidized TiN layer (25 nm TiN on a silicon substrate after wet oxidation at 400 ºC for 2 hours) for nitrogen, titanium and oxygen. Corresponding depth profiles (b) obtained from quantification and integration of the selected square areas.

3.4.3 Passivation

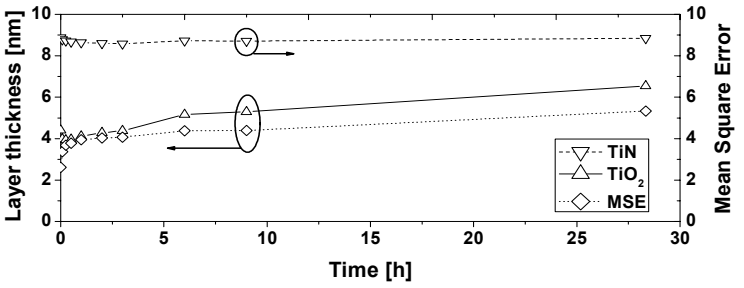
TiN samples were passivated with various passivation layers. For passivated samples, the SE model includes the extra layers for passivation on top of TiN. After deposition of the passivation layer (see section 3.2), the samples were subjected to oxidation in wet ambient at 400 ºC and 500 ºC. In Figure 3.8, the TiO_2 thickness versus time curves are shown for wet oxidation at 500 ºC, using 50 nm PECVD SiO_2 (Oxford) (Figure 3.8a), 40 nm ICPECVD SiO_2 (Figure 3.8b), 50 nm ALD Al_2O_3 (Figure 3.8c) and 25 nm ICPECVD Si_3N_4 (Figure 3.8d) as passivation layers.

Very little change in TiN and TiO_2 thickness (< 0.5 nm) and the MSE is observed, except for the (Oxford) PECVD SiO_2 sample after 3 hours of oxidation time. The increase in TiO_2 thickness indicates oxidation of the TiN layer. The increase in the MSE of the model is most likely the result of a change in the properties of the thin films as they are heated (annealed) at a temperature above the deposition temperature of the layers [60].

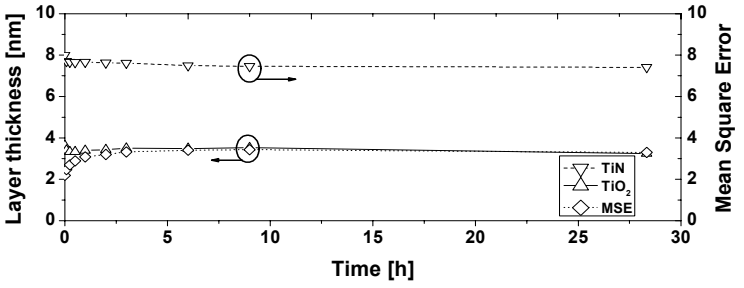
Furthermore, for the samples with a SiO_2 capping layer, a relatively thick initial TiO_2 layer (~4 nm) is observed as a result of initial plasma oxidation of the TiN layer during deposition of the capping SiO_2 layer.

For the Al_2O_3 sample, a much thinner (~0.5 nm) TiO_2 layer is found, indicating that the ALD TiN thin film is less oxidized by the deposition of the ALD Al_2O_3 capping layer than for plasma SiO_2 layers. This shows that ALD Al_2O_3 is a suitable layer to protect ALD TiN thin films during further plasma processing.

For the Si_3N_4-covered sample, the TiO_2 layer is virtually zero. This is unexpected, as prior to deposition of the Si_3N_4 layer, an ex-situ TiO_2 thickness of 1.25 nm was found. The absence of the TiO_2 layer after Si_3N_4 deposition is most likely the result of nitridation of the TiO_2 layer by the N_2-plasma [56, 105, 106]. As no significant change in all layer thicknesses is observed and the error in the fit of the optical model (MSE) does not change more than for the other samples, it is concluded that no significant oxidation has taken place for the Si_3N_4-protected sample during the oxidation experiment.



(a)



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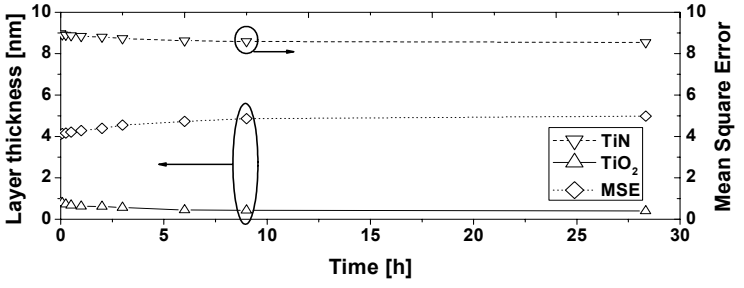
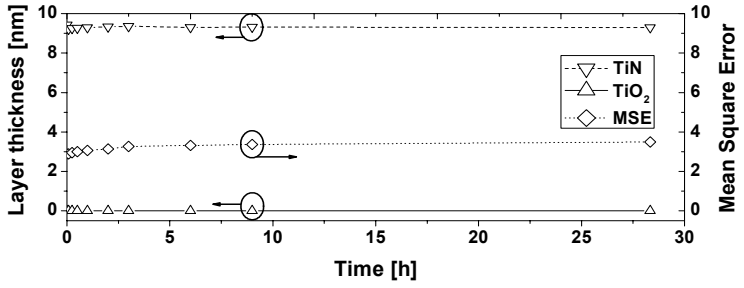


(c)



(d)

Figure 3.8: TiO_2 and TiN thickness vs time during wet oxidation at 500 ºC with the MSE of the SE model fit. 50 nm (Oxford) PECVD SiO_2 (a), 40 nm ICPECVD SiO_2 (b), 50 nm ALD Al_2O_3 (c) and 25 nm ICPECVD Si_3N_4 (d) are compared as passivation layers for ALD TiN.

It is concluded that most passivation layers can protect TiN thin films against their oxidation at 500 ºC in wet ambient up to 28 hours, except the (Oxford) PECVD SiO_2 layer. Both (IC)PECVD SiO_2 layers are less suitable for passivation, as the oxidation of TiN can occur during the first stage of the deposition process. This can be avoided by the deposition of an Al_2O_3 thin film prior to the PECVD SiO_2 deposition.

3.5 Conclusions

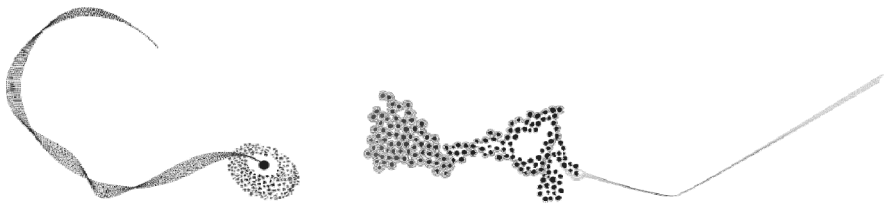
For ALD TiN layers, two regimes, initial and parabolic, are distinguished for thermal oxidation in both wet and dry ambients. For the initial regime, values of 1.1±0.1 eV and 0.9±0.2 eV are found for dry and wet oxidations respectively, and 2.0 ± 0.1 eV (dry) and 1.3 ± 0.1 eV (wet) for the parabolic regime. The extracted activation energies for the parabolic regime are in agreement with the literature values known for stoichiometric sputtered TiN layers. For plasma oxidation experiments, two time regimes are distinguished. The first very narrow regime with high oxidation rate is independent of the temperature, while for the second regime with low oxidation rate the oxidation rate increases with temperature. The existence of two regimes indicates two different oxidation mechanisms.

From the material analysis, it is shown that both as-deposited TiN and fully oxidized TiO_2 layers are stoichiometric within 10 % and contain small fractions of Cl and H. EFTEM shows decreasing N- and increasing O-concentration profiles towards the substrate across the layer thickness for the partly oxidized sample, pointing to the enhanced grain-boundary diffusion.

Passivation layers were applied to some ALD TiN samples. Samples passivated with 25-50 nm ICPECVD SiO_2 or Si_3N_4 and ALD Al_2O_3 layers showed no significant wet oxidation at temperatures up to 500 ºC for 28 hours. During plasma enhanced CVD of SiO_2, the underlying TiN oxidizes significantly during the first minute of deposition. This makes plasma-SiO_2 less suitable as passivation layer for ultrathin ALD TiN films, unless another passivation layer (for instance ALD Al_2O_3) is deposited first.

4

Design, fabrication and electrical characterization of SMAs



4.1 Outline

In this chapter, micro- and nanolink-based thermal devices ('suspended membrane actuators', SMAs) are discussed, fabricated using the 'drill-and-fill' process (see section 1.3). In the first part, the design and materials are discussed as well an electrical model of the device. Next, the fabrication ('drill-and-fill') process and the realized micro- and nanolink based SMAs are presented. In the final part, the electrical characterization of the SMAs is shown.

4.2 Design and materials

4.2.1 Design

The design of the SMA is based on antifuse-based chemical sensors and actuators by Kovalgin *et al.* [2], and consists of two crossing electrodes separated by an SiO_2 dielectric layer, as shown in Figure 4.1 and Figure 4.2. Designs with different parameters were fabricated with variations in link diameter d (2-6 μm), electrode width w (3-10 μm) and membrane size (20×20–110×110 μm^2). An example of a design parameter set for microlink-based SMAs is shown in Table 4.1. SMA-1 is the standard design, SMA-2 and SMA-3 have variations in link diameter, SMA-4 and SMA-5 have a reduced electrode width (in a small part of the electrode only: 'pinched') and

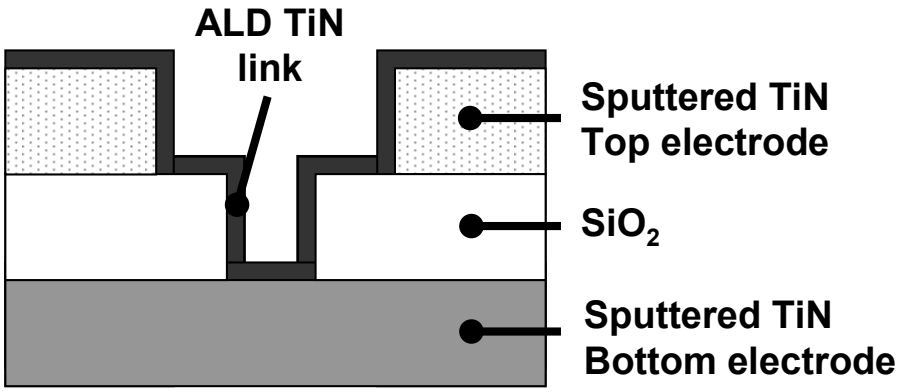


Figure 4.1: Cross-section of micro- and nanolink-based suspended membrane actuators (SMAs).

SMA-6 and SMA-7 have extremely large links. For the nanolink devices, the same design is used yet with a fixed link size of 100 nm. All devices are placed in a die together with a set of process control modules (PCMs) including SMAs without membrane or link, Greek Cross structures of top, bottom and ALD TiN electrodes as well as SEM cross-section structures (see Figure 4.3).

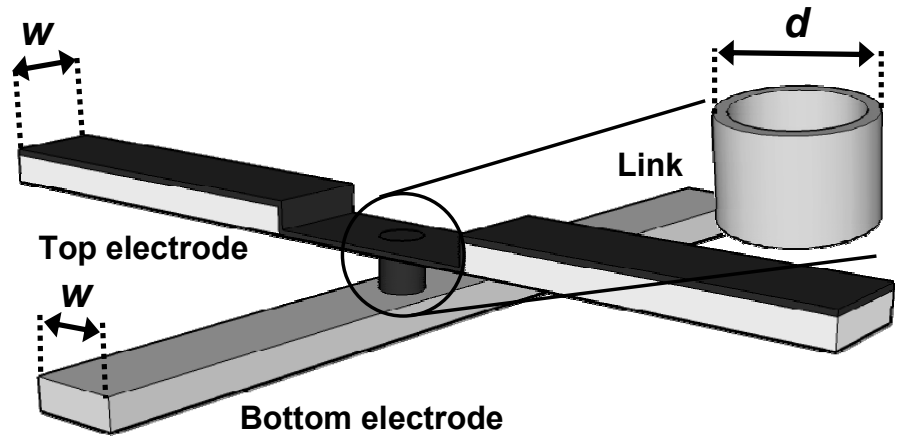


Figure 4.2: 3D impression of micro- and nanolink-based suspended membrane actuators (SMAs); "w" indicates the electrode width, "d" the link diameter.

SMA number	w_electrodes	d_link	A_link	A_membrane
	µm	µm	µm^2	µm^2
1	10	3.5	9.62	110x110
2	10	**2**	3.14	110x110
3	10	**6**	28.27	110x110
4	**3 (10 µm pinched)**	**3.5**	**9.62**	110x110
5	**3 (10 µm pinched)**	**2**	**3.14**	110x110
6	10	**23.5**	433.72	110x110
7	10	**89**	6220.96	110x110

Table 4.1: Design variations for microlink-based SMAs with different electrode width (w_electrodes), link diameter (d_link), link area (A_link) and membrane area (A_membrane).

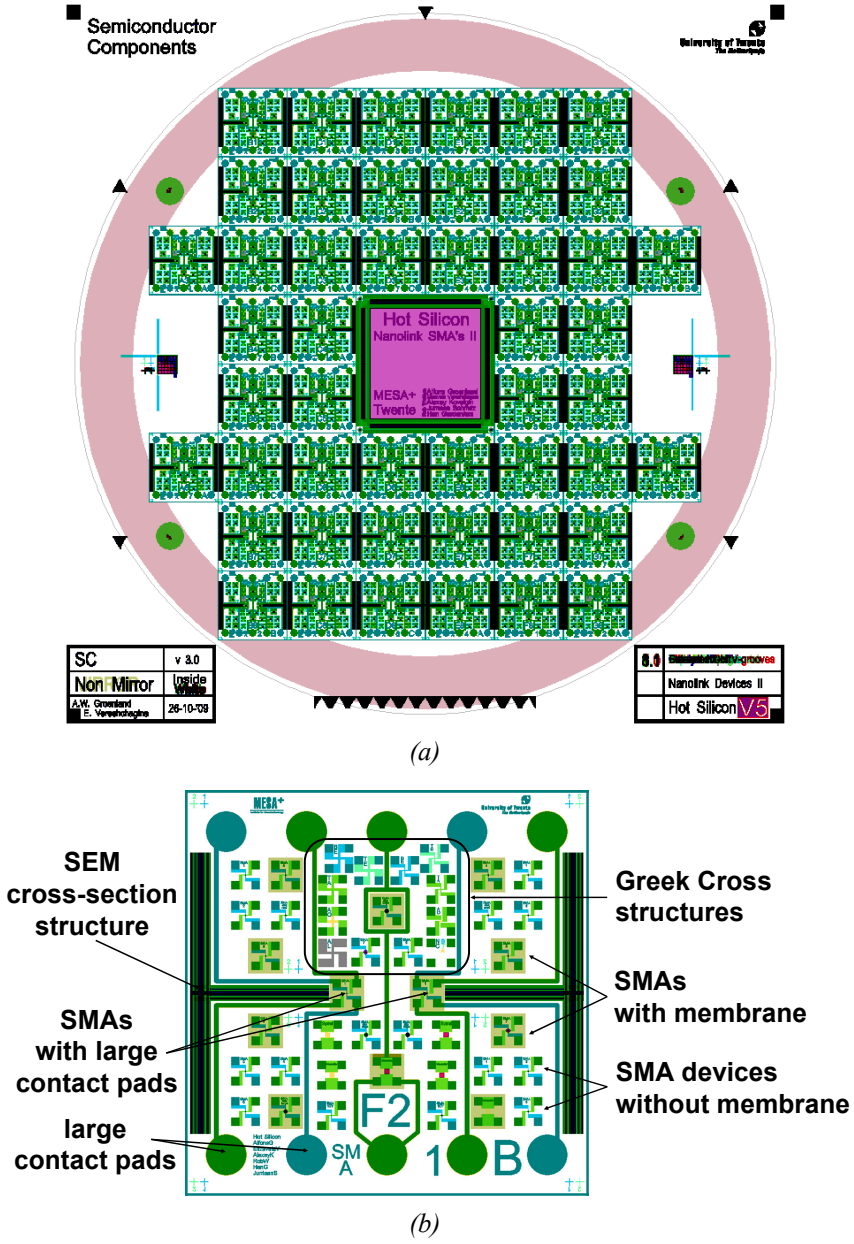


Figure 4.3: *(a) Mask design of a 100 mm wafer with 48 dies of 1×1 cm. (b) Die with SMAs and process control modules (PCMs) such as Greek Cross and SEM cross-section structures.*

4.2.2 Materials

Titanium nitride (TiN) is used as material to make the link and the connection electrodes (see section 1.3.1). TiN is selected as material because of its electrical properties (ρ and TCR), CMOS compatibility, the deposition process by ALD and the good gap filling properties. The ALD TiN layer is *in situ* (without vacuum break) covered by a 15 nm Al_2O_3 and 100 nm SiO_2 passivation stack to protect it from oxidation at elevated temperatures.

The top and bottom electrode are fabricated from 100 nm sputtered TiN (see Figure 4.2). The (thicker) sputtered TiN layer lowers the series resistance of the top electrode.

SiO_2 is selected as dielectric material because of its good dielectric properties (low leakage currents, high breakdown field) in combination with good (plasma) etching properties [39].

4.2.3 Electrical model

The low power electrical and thermal behaviour of the SMAs is, apart from good thermal insulation by using a freely etched SiRN membrane, attributed to the high ratio between the link resistance (R_{link}) and the connection electrodes (R_{con}) (see section 1.2.2). The electrical behaviour of the SMA can be described, in first order approximation, as a resistor network of the link (R_{link}) and top (R_{TE}) and bottom (R_{BE}) electrodes. This is schematically shown in Figure 4.4a. The link resistance is defined as the measured total resistance between the top and bottom electrode (which also referred to as R_{diff}, see section 4.5.1). The link resistance consists of the resistance of the cylindrically shaped ALD TiN layer (R_{cyl}) in series with the (metal-to-metal) contact resistance (R_{cont}) of the ALD TiN cylinder to the bottom electrode (Figure 4.4b).

The ALD TiN cylinder resistance is determined by the cylinder geometry and it can be approximated as

$$R_{cyl} = \rho_{TiN}\frac{l_{link}}{A_{link}} = \rho_{TiN}\frac{l_{link}}{\pi((\frac{D_{link}}{2})^2 - (\frac{D_{link}}{2} - t_{TiN})^2)} \qquad (4.1)$$

where ρ_{TiN} is the ALD TiN resistivity [Ωcm], l_{link} is the link height [cm], and A_{link} is the (top) surface area [cm^2] of the cylinder having a diameter (D_{link}) [cm]. t_{TiN} is the thickness [cm] of the ALD TiN layer (see inset of Figure 4.5).

For metal-to-metal contacts, the contact resistance is a function of the link diameter only [67]

$$R_{cont} = \frac{\rho_c}{A_{link}} = \frac{\rho_c}{\pi(\frac{D_{link}}{2})^2} \tag{4.2}$$

where ρ_c is the specific contact resistance [Ωcm^2].

In Figure 4.5, calculated values for R_{cyl} and R_{cont} are shown as a function of the link diameter for 5, 8 and 16 nm ALD TiN and ρ_c values in the range of 10^{-7} to 10^{-9} Ωcm^2. These are realistic values for good metal-to-metal contacts [107, 108].

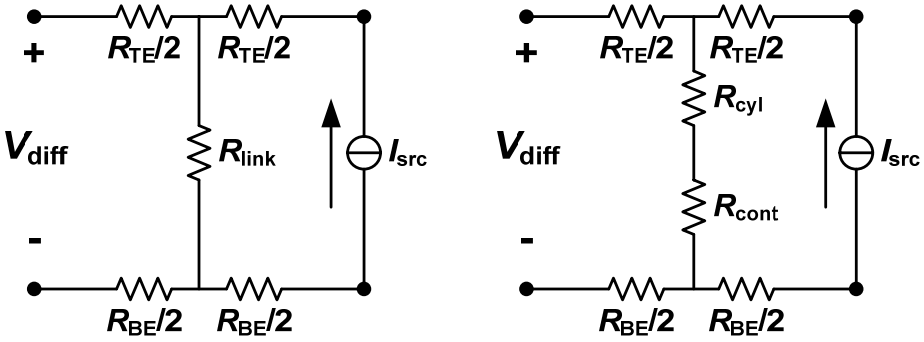


Figure 4.4: (a) Electrical model of the SMA with the measured link resistance (R_{link}), top (R_{TE}) and bottom (R_{BE}) electrode.
(b) Electrical model with the link resistance replaced by the resistance of the ALD TiN cylinder (R_{cyl}) in series with the (metal-to-metal) contact resistance (R_{cont}) to the bottom electrode.

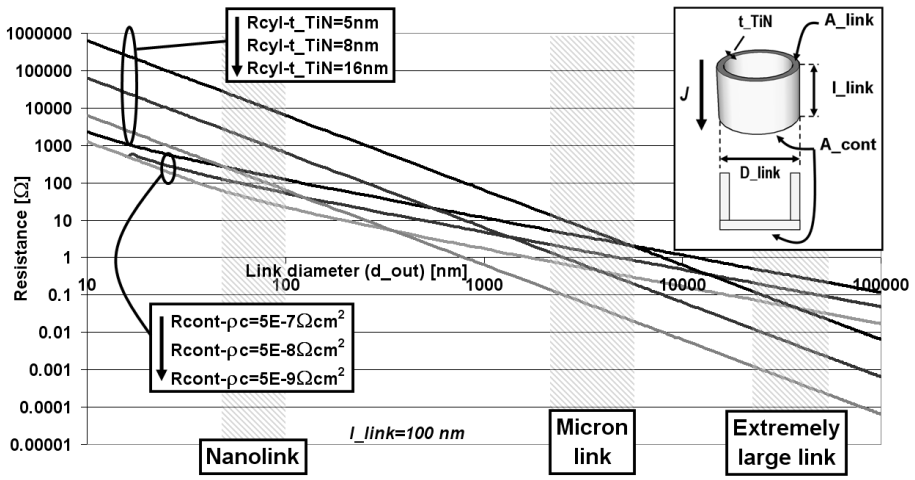


Figure 4.5: Calculated ALD TiN cylinder resistance (R_{cyl}) and the contact resistance (R_{cont}) as a function of link diameter for 5, 8 and 16 nm ALD TiN layers and specific contact resistance values in the range of 10^{-7}-10^{-9} Ωcm^2. Marked areas indicate approximate link dimensions of nanolink, microlink and extremely large links. Inset shows a 3D impression and cross-section of the ALD TiN cylinder/link.

The calculations, based on eq. (4.1) and (4.2), show that for microlinks (∅ 1-10 μm) both cylinder and contact resistance are in the same order of magnitude. A total link resistance in the range of 10^1-10^3 Ω is expected. For nanolinks (∅ 50-100 nm), the link resistance is dominated by the contact resistance and is independent of the ALD TiN cylinder resistance. The link resistance is in the range of 10^4-10^6 Ω depending on the specific contact resistance. For extremely large links (∅ 10-100 μm), the link resistance is determined by the cylinder resistance only and it is extremely low (< 1 Ω).

4.3 Fabrication

4.3.1 Microlink-based SMAs

Starting from standard low doped (10^{15} cm^{-3} B) *p*-type <100> silicon wafers, the first process step is the deposition of 100 nm low stress silicon (rich) nitride (SiRN) via low pressure chemical vapour deposition. Subsequently a layer of 100 nm titanium nitride is deposited via reactive sputtering of titanium in an Ar/N_2 mixture. It is patterned using wet chemical etching in a mixture of hydrogen peroxide and ammonia to become the bottom electrode (Figure 4.6a). The bottom electrode is covered with 100 nm silicon oxide via plasma enhanced chemical vapour deposition (PECVD) (Figure 4.6b). Next, again 100 nm of TiN is deposited and patterned to become the thick part of the top electrode. The processing is similar to the bottom electrode (Figure 4.6c). Then, the hole for the link is etched in the SiO_2 layer in the centre of the structure using a CHF_3-based reactive ion etching process (Figure 4.6d). The micron sized hole is fabricated with standard UV lithography, while for the nanoscopic hole e-beam lithography (see section 4.3.2) is used. After a sputter etch in argon (argon bombardment) to clean the bottom of the hole for the contact to the bottom electrode, a 7 nm (for the microlink) or a 15 nm (for the nanolink) TiN layer is deposited via ALD without vacuum break to make the link. The TiN thin film is covered (for protection or 'passivation') by 15 nm Al_2O_3 and 50 nm of ICPECVD SiO_2 without vacuum break. Next, the ALD TiN thin film and passivation stack are patterned using wet chemical etching in a solution of hydrogen peroxide (H_2O_2) + ammonia (NH_3) and hydrofluoric acid (HF), respectively (Figure 4.6e). After deposition of a second 50 nm SiO_2 passivation layer, vias are etched towards the TiN electrodes using HF, and filled with 1 μm aluminum to become contact pads (Figure 4.6f).

Aluminum with patterned by standard H_3PO_4-based wet chemical etchant at 60 ºC. In the final step, the SiRN membrane is released from the backside using wet chemical etching in 25 % KOH at 75 ºC, for which the SiRN layer on the backside of the wafer as a hard mask (Figure 4.6g).

During KOH etching, the frontside of the wafer is protected using a stainless steel wafer holder with rubber O-rings, such that only the backside of the wafer is exposed to the etching solution. Optical micrographs of a realized SMA with microlink are shown in Figure 4.7.

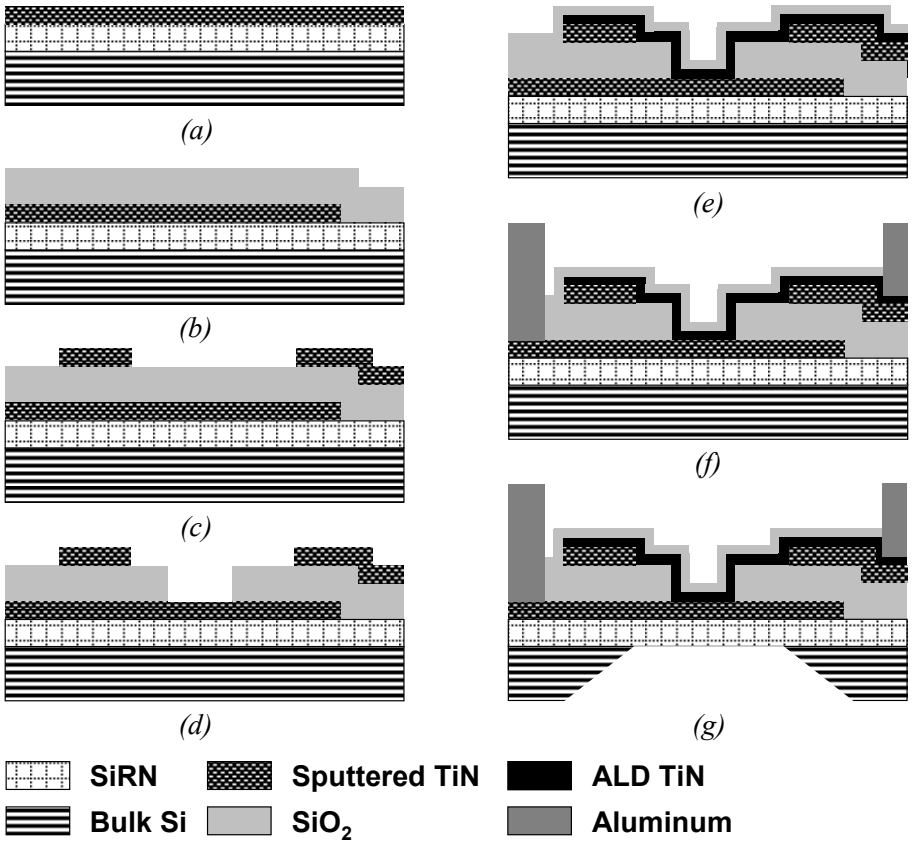
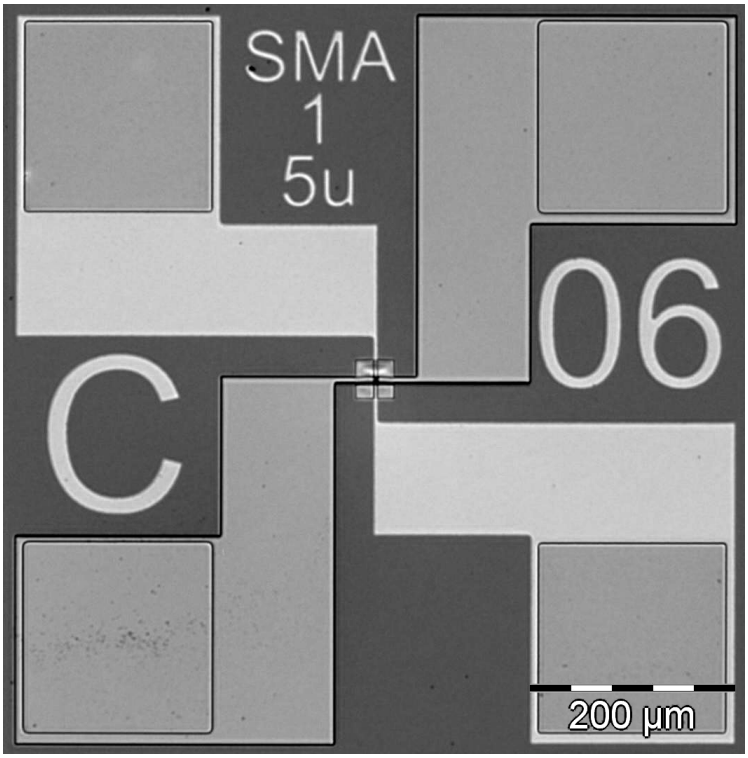
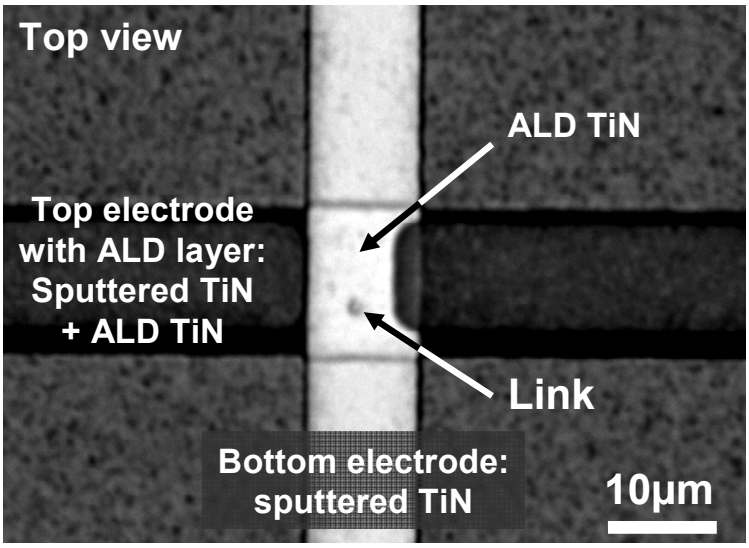


Figure 4.6: Fabrication scheme for SMAs.



(a)



(b)

Figure 4.7: Optical micrographs of a realized microlink-based SMA.verview (a) and close-up of the centre with the microlink (b).

4.3.2 Nanolink-based SMAs

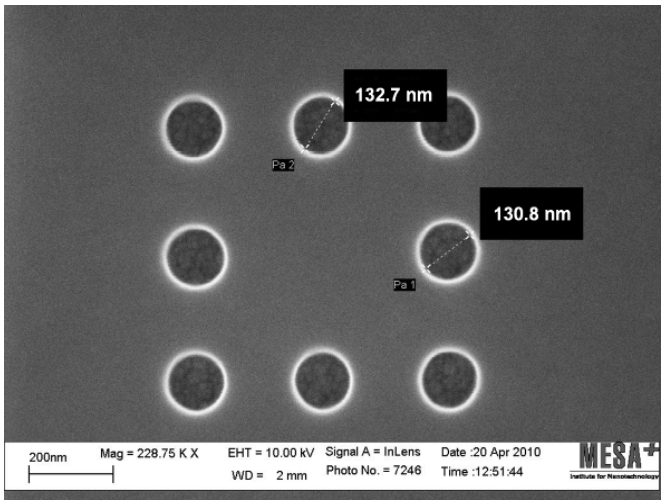
For fabrication of the nanolink-based SMA, the same fabrication process as for the microlink-based SMAs is used, except for the link (i.e. nanohole) definition step, for which e-beam lithography is used. The latter is is described in more detail in this section.

Starting from Figure 4.6c, after patterning of the TiN top electrode patterning, ZEP520A resist (negative tone, Zeon Europa) is used to define the nanoholes. A ~100 nm layer of ZEP resist, diluted with anisole ($CH_3OC_6H_5$) (1:1), is spun on the wafer at 500 rpm for 5 s and at 2500 rpm for 55 s, followed by a prebake at 180 ºC for 3 min. Next, nanoholes are written in the resist by single pulse e-beam exposure with a dose of 10000 $\mu C/cm^2$. The pattern is aligned to predefined topographic alignment structures, which resulted in an alignment accuracy of the holes within 2 μm with respect to the top and bottom electrode. The layer is developed in a solution of n-amylacetate (Merck 8.18700.1000) for 90 s and rinsed in a mixture of IPA (2-propanol) and Methyl-Isobutyl-Kethone (MIBK) (IPA:MIBK 9:1). With this procedure, holes in the ZEP resist with a diameter of 130 nm were obtained (see Figure 4.8a).

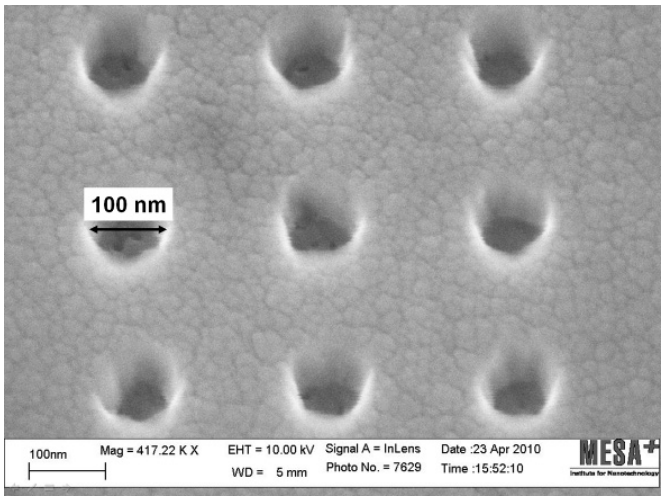
Subsequently, the holes are etched in the underlying SiO_2 layer by using RIE in pure CHF_3 at a pressure of ~4 mTorr. After etching, the ZEP resist is removed in a two-step process: first softening the resist by an ultra violet (UV) exposure of 1800 mJ/cm^2 and secondly, stripping it in a 100 % HNO_3 for 30 min. In Figure 4.8b, the resulting holes in the SiO_2 layer with a diameter of 100 nm are shown.

After application of the remaining process steps (see the microlink-based SMA fabrication, section 4.3.1), the nanolink-based SMA is realized. A top-view image of a device with a membrane is shown in Figure 4.9a. In Figure 4.9b, an HRSEM image with a close-up of the centre of the device is shown. The nanolink is positioned within an offset of ~2 μm from the centre of the central rectangular area.

In Figure 4.9c, a focussed ion beam (FIB) cross-section through the nanoscopic hole is shown. One can see that the hole is completely etched through the SiO_2 layer and filled with the ALD TiN layer that perfectly follows the topography. A thin interfacial layer is observed between the ALD TiN layer and the (sputtered) TiN bottom electrode.

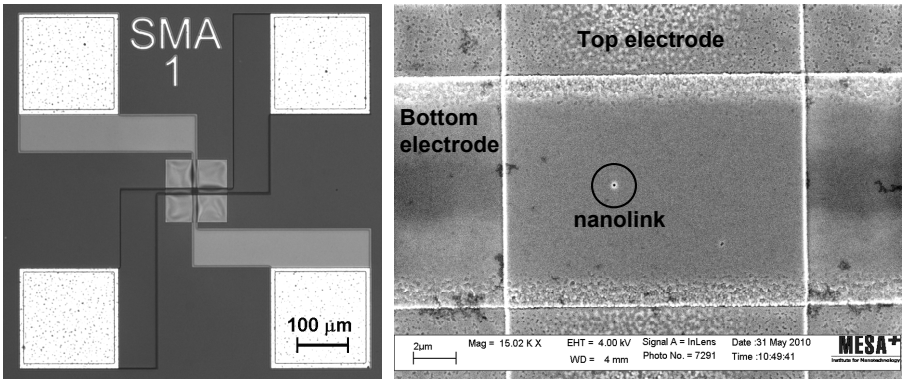


(a)

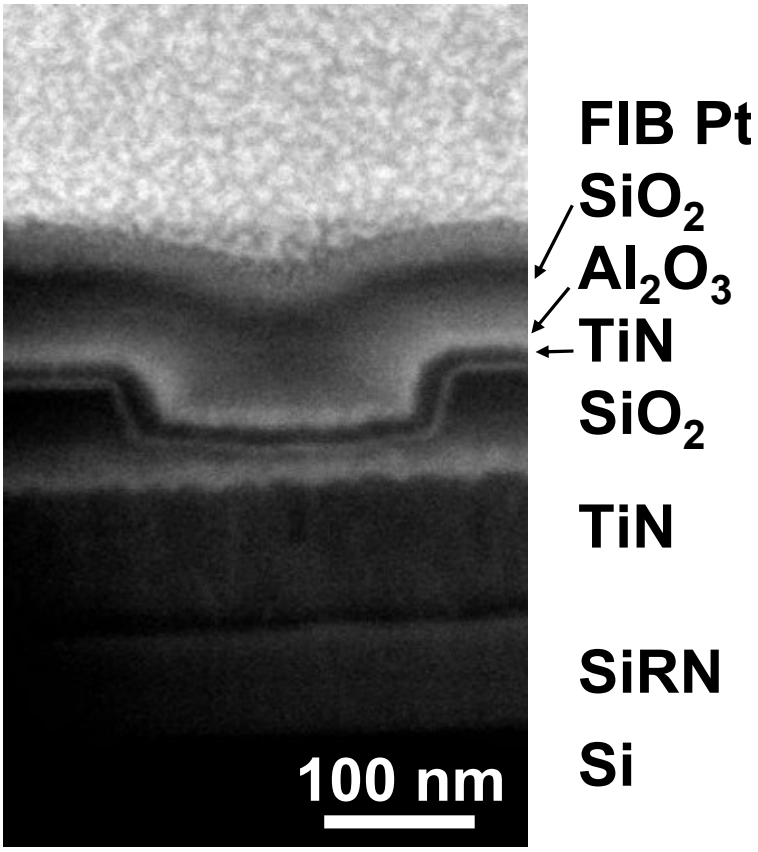


(b)

Figure 4.8: SEM images showing a test pattern with nanoholes in ZEP resist before the RIE etch (a) and in the SiO_2 layer after the RIE and resist strip (b).



(a) *(b)*



(c)

Figure 4.9: (a) Optical micrograph of a nanolink-based SMA.
(b) HRSEM image showing the centre of the SMA with nanolink.
(c) FIB cross-section through the nanolink.with an additional platinum layer on top, necessary for the FIB process.

4.4 Experimental

The layer thickness of the ALD TiN films is determined using a Woollam M2000 Spectroscopic Ellipsometer (SE) in the energy range 0.7-5 eV. Measurements were taken *in situ* directly after deposition (see section 1.3.3). From the recorded SE data, the ALD TiN layer thickness is derived using a model containing the optical constants of all sub-layers (see section 3.3). For the electrical characterization, *IV*-measurements are carried out using a HP4156B or Keithley 4200 precision semiconductor parameter analyzer in combination with a Cascade Microtech, Karl Süss PM8 or Süss Microtech PA200 probe station. For the temperature calibration measurements, the temperature controlled chuck of the probe station (Cascade Microtech or Süss Microtech PA200) is used.

4.5 Results: electrical characterization

4.5.1 Metrology

SMAs were characterized before and after the final KOH-based membrane release etch. The devices are electrically characterized using a four-point metrology. A voltage (V_{src}) is forced between two adjacent electrodes, leading to a current through the link (I_{src}). The link resistance is measured without the electrode resistance (see section 2.2.2), by measuring the voltage drop (V_{diff}) over the two opposite electrodes (Figure 4.10); the four-point link resistance (R_{link}, or *differential* resistance, R_{diff}) is calculated as $R_{diff} = V_{diff} / I_{src}$.

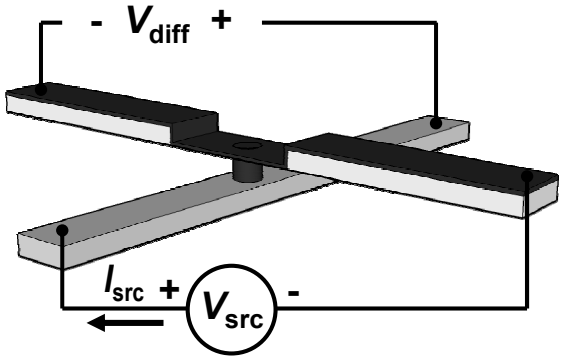


Figure 4.10: Setup for electrical characterization of SMAs.

4.5.2 Microlink-based SMAs

4.5.2.1 Non-suspended membrane

Devices with a microlink are characterized using the four-point metrology, prior to the final membrane release etch. V_{diff} versus I_{src} (shortly *IV*-) characteristics are shown in Figure 4.11 for temperatures in the range of 25-175 ºC. Linear *IV*-behaviour is observed for all temperatures. A link resistance (R_{diff}) of 39.9 Ω is extracted from the slope of the *IV*-characteristic at 25 °C. In Figure 4.12 R_{diff} is plotted as a function of temperature. From the slope and the (extrapolated) intercept at 0 ºC (R_0), the temperature coefficient of resistance (TCR, see section 2.2.4) is calculated to be 2.9×10^{-4} /ºC. For comparison, resistance values of the flat ALD TiN layer, measured by a Greek Cross test structure on the same wafer, are also plotted in Figure 4.12. From the GC data, a TCR of 3.3×10^{-4} /ºC is found. This is in agreement with the TCR of 7 nm ALD TiN layers ($3.0\text{-}3.5\times10^{-4}$ /°C), shown in chapter 2, section 2.4.5.1. The TCR of the microlink and that of the flat ALD TiN layer are in good agreement. In this respect, the hollow cylinder-shaped ALD TiN layer behaves similar to the flat ALD TiN layer.

It is concluded for microlink-based SMAs that the total link resistance is dominated by the resistance of the ALD TiN layer (R_{cyl}) and thus that the contact resistance is negligible (see Figure 4.4).

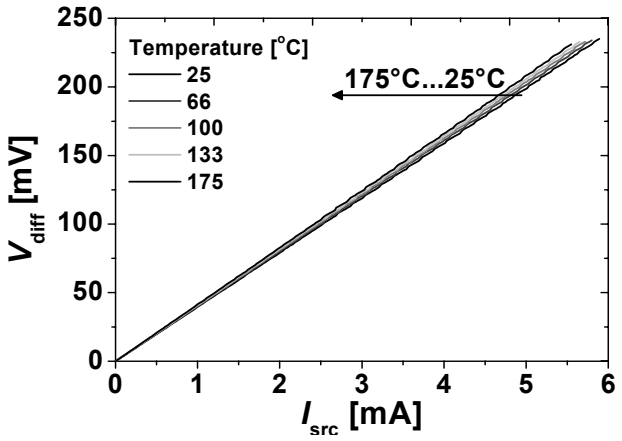


Figure 4.11: V_{diff} vs I_{src} for a non-suspended microlink-based SMA for temperatures in the range of 25-175 ºC.

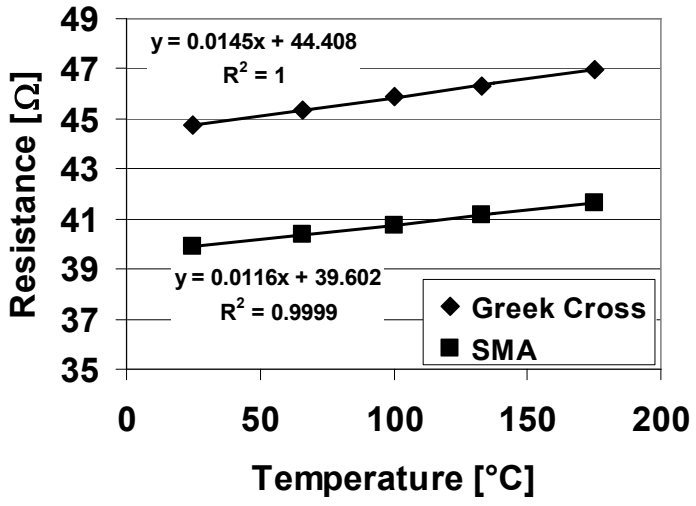


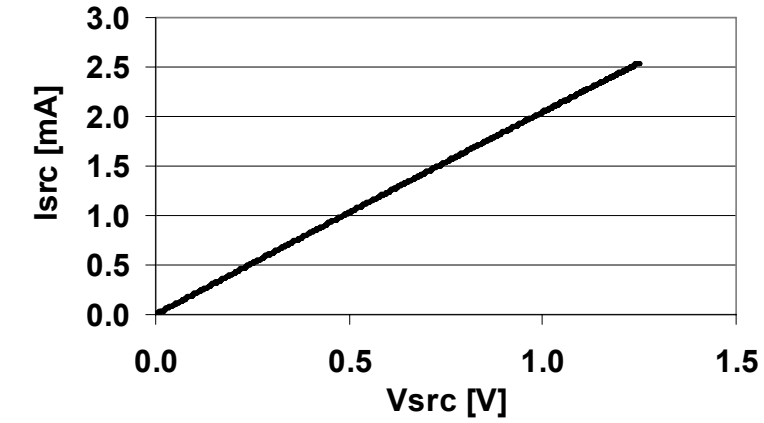
Figure 4.12: (Link) resistance vs temperature for a non-suspended microlink-based SMA and a Greek Cross of the same (flat) ALD TiN layer. Lines are linear fits through the data. TCR values of 3.3×10^{-4} /°C and 2.9×10^{-4} /°C are extracted from the linear fits for the SMA and GC device, respectively.

4.5.2.2 Suspended membrane

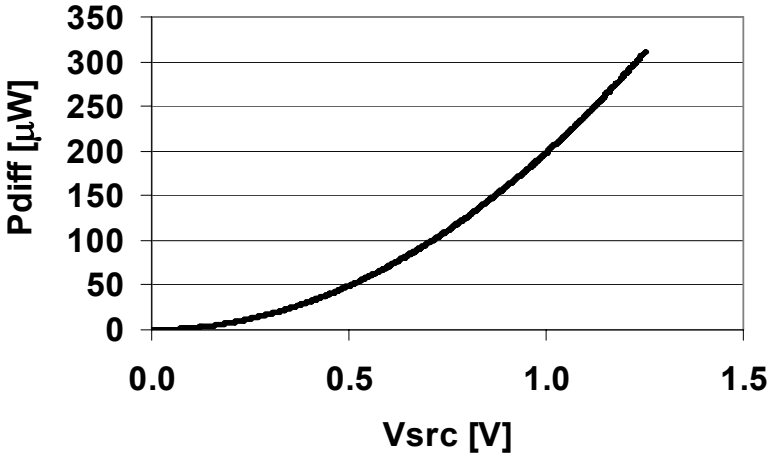
Next, the membrane release etch is carried out and *IV*-characteristics are measured on suspended SMAs. In Figure 4.13a, V_{src} versus I_{src} is shown. A linear *IV*-behaviour is observed in the entire voltage range. A link resistance of 46.0 Ω at 25 ºC is extracted. Next, the power consumed in the link is calculated as $P_{diff} = V_{diff} \cdot I_{src}$ and plotted versus V_{src} in Figure 4.13b. At 1.25 V, 310 μW is dissipated in the link. Subsequently, the link resistance (R_{diff}) is plotted versus the P_{diff} in Figure 4.14a. A linear dependence is observed between the link resistance and the power consumed in the link.

From the change in the resistance, the temperature can be calculated using R_0 (45.7 Ω) and the TCR of 2.5×10^{-4} /°C (see eq. (2.12), section 2.2.4). The TCR is slightly lower than the values measured for other devices ($3.0\text{-}3.5\times10^{-4}$ °C). This might be related to variations of the ALD TiN resistivity across the wafer, as shown in section 2.4.4. The temperature versus the power consumed in the link is shown in Figure 4.14b and

compared with data of the (same) device prior to the membrane release etch. For the suspended device, a little hysteresis is observed. This might be a result of the non-zero thermal mass of the device. It is observed that a link temperature of ~200 ºC can be achieved with a power consumption of ~0.3 mW. The device without suspended membrane exhibits almost no heating. This confirms the significance of releasing the membrane on efficient heating in micro-link based SMAs.

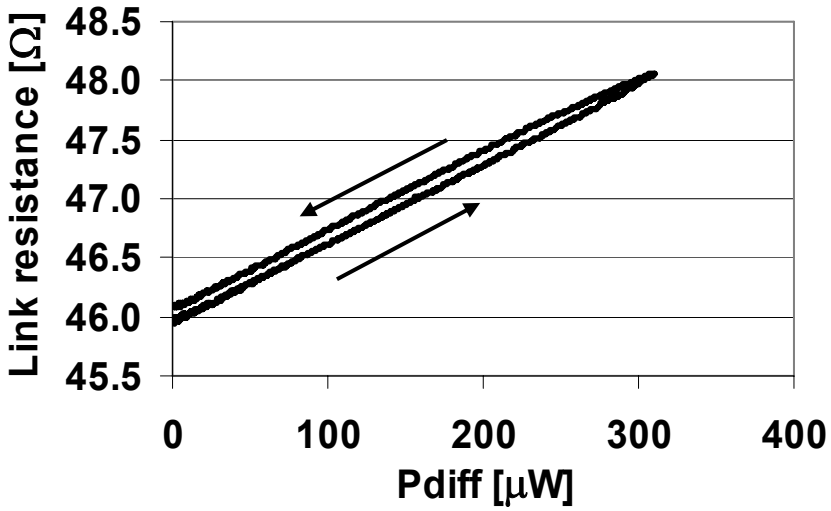


(a)

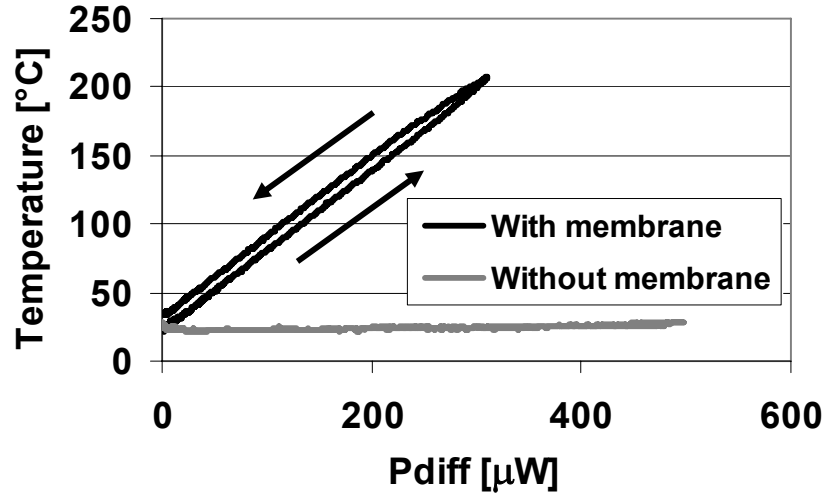


(b)

Figure 4.13: I_{src} vs V_{src} (a) and P_{diff} vs V_{src} (b) for a suspended microlink-based SMA.



(a)



(b)

Figure 4.14: R_{diff} vs P_{diff} (a) for a suspended microlink-based SMA. Corresponding temperature vs P_{diff} (b) data of the device before ('without membrane') and after ('with membrane') the membrane release etch. The temperature is calculated from the resistance change (see eq. (2.12)) using an R_0 value of 45.7 Ω and a TCR of 2.5×10^{-4} /ºC.

4.5.3 Nanolink-based SMAs

4.5.3.1 Non-suspended membrane

SMAs with a nanolink were characterized prior to the final membrane release etch. For a nanolink-based SMA, V_{diff} versus I_{src} characteristics are shown in Figure 4.15 for temperatures in the range of 25-300 ºC. A linear *IV*-behaviour is observed for all temperatures. A link resistance of 7 MΩ is extracted from the slope of the *IV*-characteristic at 25 °C. In Figure 4.16, R_{diff} is plotted for all temperatures. In a first approximation, a linear function is fitted through the data with a good fit ($R^2 > 0.95$). From the slope of the fitted line and R_0, the TCR is calculated as -3.3×10^{-3} /ºC. The TCR is negative and an order of magnitude higher in absolute terms than the TCR of the microlink and the flat ALD TiN layer (~$2.9\text{-}3.3\times10^{-4}$ /°C, see Figure 4.12). Given the high resistance of the nanolink compared to the microlink, and the estimated resistance of the ALD TiN cylinder (R_{cyl}), the contact resistance (R_{cont}), is dominating in this configuration (see the model in section 4.2.3). Using eq. (4.2) and neglecting the ALD TiN cylinder resistance, the specific contact resistance for the ∅ 100 nm nanolink is calculated as approximately 5.5×10^{-4} Ωcm^2. This is a very high value [55]

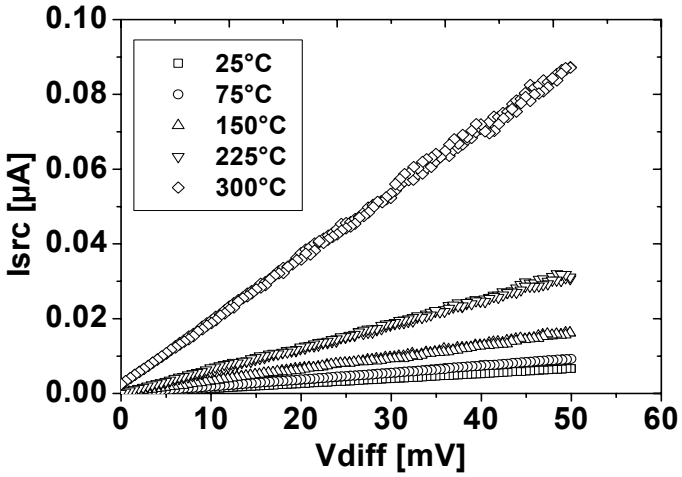


Figure 4.15: I_{src} vs V_{src} for a non-suspended nanolink-based SMA for temperatures in the range of 25-300 ºC.

and is most likely the result of the interfacial layer between the nanolink and the bottom electrode (see Figure 4.9c). Contact resistances are known to exhibit a negative TCR as result of a decreasing barrier at elevated temperatures [109].

It is concluded that for nanolink-based SMAs the total link resistance is dominated by the contact resistance, and not by the resistance of the ALD TiN layer. This is opposite to the link resistance of microlink-based SMAs.

4.5.3.2 Suspended membrane

Next, the membrane release etch is carried out and *IV*-characteristics are measured on a suspended nanolink-based SMA. In Figure 4.17a, V_{src} versus I_{src} is shown. Nonlinear behaviour is observed in the given voltage range. Next, P_{diff} is shown versus V_{src} in Figure 4.17b. At V_{src} = 2.0 V, a power of 5.1 µW is dissipated in the link. In Figure 4.18a, the link resistance R_{diff} is plotted versus the power dissipated in the link. From the change of the resistance, the TCR and R_0, the $T(P_{diff})$-curve is calculated and plotted in Figure 4.18b. It is observed, a link temperature of ~280 ºC can be achieved with a power dissipation of ~5 µW in the link for this device and 200 ºC with 0.5 µW. This is more than 2 orders of magnitude lower than for the microlink-based SMA (200 ºC with ~0.3 mW) and for the antifuse-based SMAs by Kovalgin *et al.* (200 ºC at ~0.3 mW) [2].

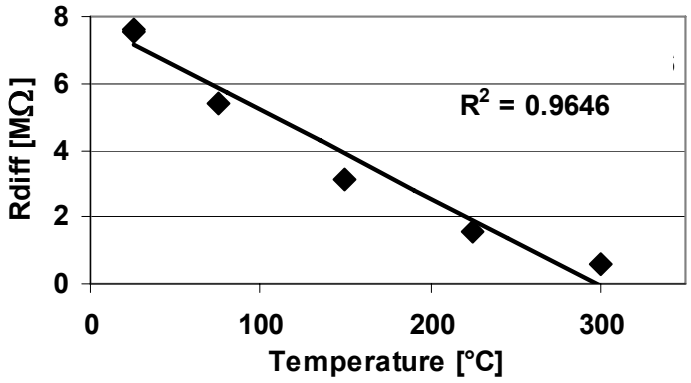
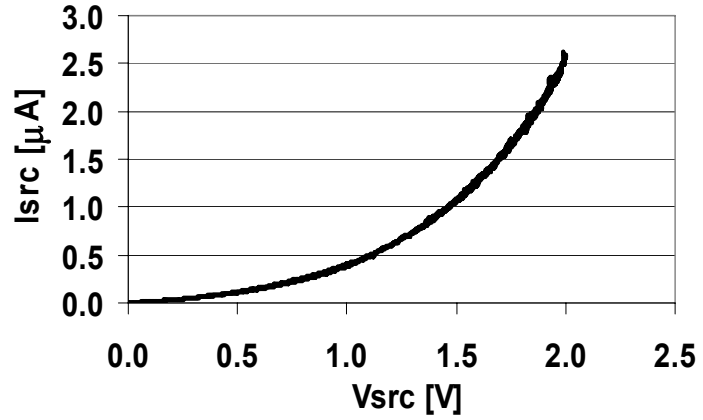
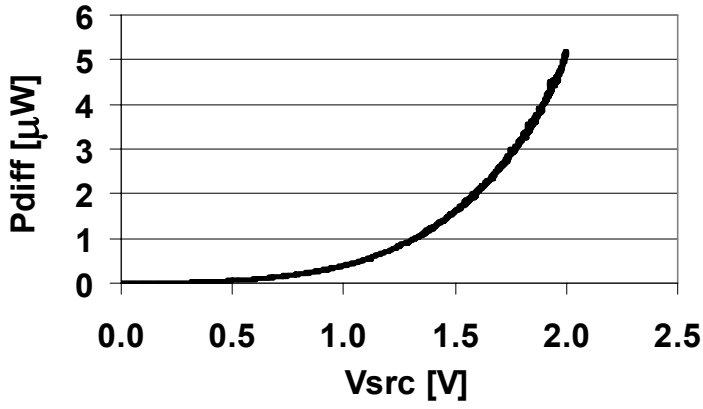


Figure 4.16: Resistance vs temperature for a non-suspended nanolink-based SMA including a linear fit through the data. The extracted temperature coefficient of resistance is -3.3×10^{-3} /ºC.

Furthermore, a parabolic shape is observed in the $T(P_{diff})$-curve, which is different from the linear behaviour in the $T(P_{diff})$-curve of the microlink-based SMA (see Figure 4.14b). This is attributed to a different ratio between the power generation in the link and heat losses via the electrodes: in the nanolink much less heat is generated compared to the microlink, while the losses via the electrodes are equal. This leads to saturation at a lower temperature for the nanolink as result of the relative large heat leakage, while for the microlink only the first (steep) part of the $T(P_{diff})$-curve is observed.



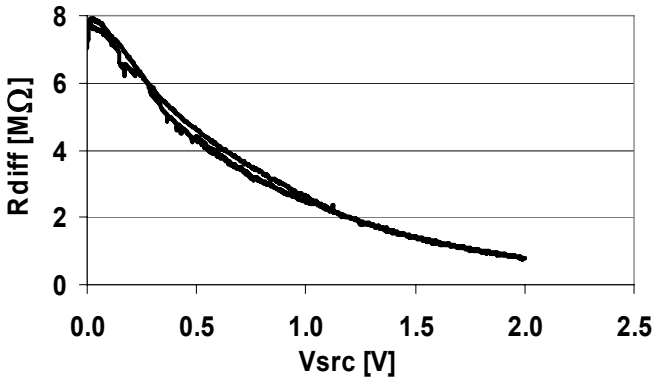
(a)



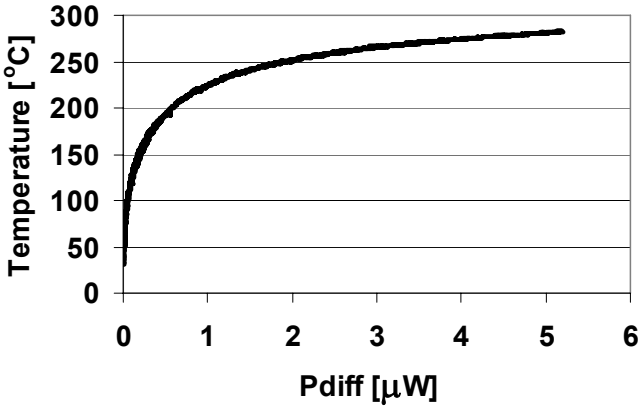
(b)

Figure 4.17: I_{src} vs V_{src} (a) and P_{diff} vs V_{src} (b) for a suspended nanolink-based SMA.

For nanolink-based SMAs, the effect of the membrane release etch is investigated by the comparison of two devices with identical design, comparable link resistances, that are fabricated at the same wafer (but different from the devices described in section 4.5.2.1) and which are positioned at approximately the same location at the wafer. For the non-suspended nanolink-based SMAs (R_{link} at 25 ºC = 5.0 kΩ) and suspended SMAs (R_{link} at 25 ºC = 4.4 kΩ) and TCR values of both -7.6×10^{-4} /ºC, $T(P_{diff})$-curves are shown in Figure 4.19. Similar parabolic $T(P_{diff})$-behaviour is observed.



(a)



(b)

Figure 4.18: R_{diff} vs V_{src} (a) and temperature vs P_{diff} (b) for a suspended anolink-based SMA.

For a power dissipation in the link of 0.2 mW, link temperatures of ~265 ºC and ~348 ºC are observed for non-suspended and suspended SMAs, respectively. Or, in other words, a link temperature of 250 ºC is obtained with 0.16 mW and 0.07 mW for non-suspended and suspended SMAs, respectively.

This result shows that releasing the membrane has much less effect on the link temperature of a nanolink- compared to microlink-based SMAs, indicating that the heating in the nanolink-based SMA is very local. Furthermore, for nanolink-based SMAs, the (cumbersome) membrane etch can be omitted for temperatures up to 265 ºC at the cost doubling the power dissipation in the link. This simplifies the fabrication process [110].

Omission of the membrane etch can increase the lifetime of nanolink-based thermal sensors and actuators, since rupture of the SiRN membrane is an important root-cause for limited lifetime of low-power suspended-membrane-based thermal sensors and actuators [111, 112]. Higher link temperatures can be achieved by reducing the heat loss towards the substrate by the fabrication of nanolink-based SMAs on quartz (SiO_2) substrates; the thermal conductivity of quartz (~1.3 W/m·K) is 2 orders of magnitude lower than that of silicon (~1.5×10^2 W /m·K) [77].

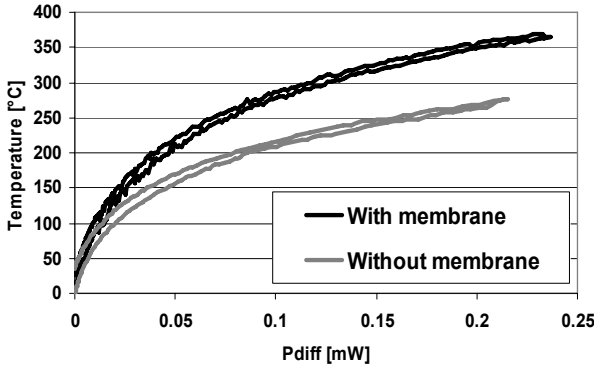


Figure 4.19: Temperature vs P_{diff} for a nanolink-based SMA with and without suspended membrane. The temperature is calculated from the resistance change (see eq. (2.12)) using the R_0 values of 5.0 kΩ and 4.4 kΩ for devices without and with suspended membrane, respectively, and the TCR of -7.6×10^{-4} /ºC for both devices.

4.6 Conclusions

Low-power thermal devices are presented (suspended membrane actuators, SMAs) based on Joule heating of a small conductive volume (link), sandwiched between two electrodes. The link is fabricated by etching a hole in the dielectric layer between the electrodes and subsequently filling it with TiN deposited via ALD ('drill-and-fill process'). This results in a hollow vertical cylinder with the walls covered by a conductive (TiN) film with a thickness of 7-15 nm.

Devices with micro- (∅ ~1 μm) and nanolinks (∅ ~100 nm) were fabricated on Si substrates with and without releasing the SiRN membrane. Electrical characterization of the devices in terms of the link resistance (R_{link}) is discussed using a model, consisting of the resistance of the (cylindrically shaped) ALD TiN film (R_{cyl}) and the (metal-to-metal) contact resistance of the ALD TiN film with the bottom electrode (R_{cont}). The link temperature as a function of the power dissipated in the link was estimated based on the change in link resistance and the TCR.

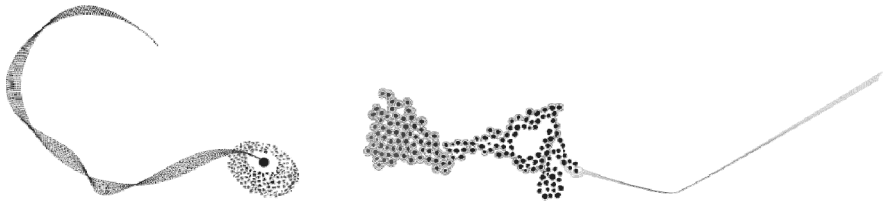
Microlink-based SMAs have low Ohmic links (~39.9-46.0 Ω) with a positive TCR (~2.5-2.9 $\times 10^{-4}$ /ºC). The link resistance is dominated by R_{cyl}. After releasing the membrane, a link temperature of ~250 ºC can be reached with a power consumption in the link of 2.7 mW. Devices without suspended membrane showed no significant heating.

Nanolink-based SMAs exhibit high Ohmic links (R_{link} 7 MΩ) with a negative TCR (-3.3×10^{-3} ºC). The link resistance is dominated by R_{cont}. Devices with suspended membrane showed link temperatures of ~280 ºC by consuming only 5.5 μW. This is more than 2 orders of magnitude lower than microlink-based SMAs, and previously reported antifuse-based SMAs of Kovalgin et.al [2].

The membrane release etch has much less effect on the link temperature for nanolink- than microlink-based SMAs. For a link temperature of 250 ºC, the power consumption is only a factor two higher than for SMAs without suspended membrane, suggesting local heating of the link.

5

Alternative temperature measurement techniques for SMAs



5.1 Outline

In chapter 4, the temperature of the micro- and nanolink-based SMAs is determined primarily from the temperature dependence of the electrical link resistance (Figure 4.14b and Figure 4.18b). In this chapter two other techniques, i.e. infrared (IR) thermometry (section 5.2) and polymer melting (section 5.3), are explored to determine the temperature of SMAs in an alternative way.

Furthermore, for some devices, a large-area platinum disk is placed on top of the device. The platinum disk makes the surface temperature more uniform and can be used additionally as catalyst for application of the SMA in pellistor type gas sensors (see section 1.2.1). Therefore, the IR thermometry technique is applied to measure the (surface) temperature of the devices with and without a platinum disk.

5.2 IR Thermometry

An object emits electromagnetic radiation according to its temperature [113]. The peak intensity of this electromagnetic radiation is a function of the temperature and is positioned at a wavelength in the infra red (IR) regime (0.78-1000 μm). Measurement of the IR radiation can be used for determination of the temperature of an object [114, 115].

5.2.1 Theory

For an ideal object or "black body", the spectral emissive power (E_b, [W/m^2/m=W/m^3]) is a function of the wavelength (λ, [m]) and the temperature (T, [K]) and is defined by Planck's law [114]:

$$E_b(\lambda,T)=\frac{C_1}{\lambda^5[\exp(C_2/\lambda T)-1]} \qquad (5.1)$$

where C_1 is the first radiation constant (3.7417749×10^{-16} W·m^2) and C_2 is the second radiation constant (0.01438769 m·K). The spectral emissive power E_b is shown as a function of wavelength for several temperatures in Figure 5.1.

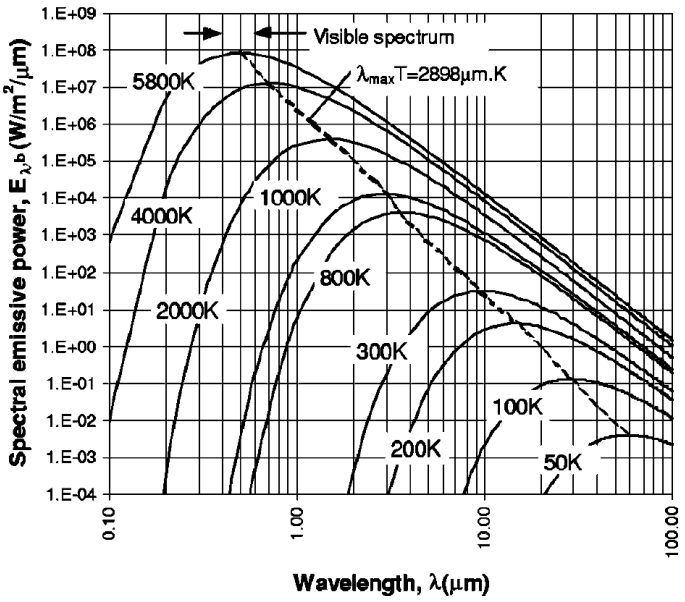


Figure 5.1: Planck's distribution for various temperatures. The line indicates the peak-power position as a function of the temperature: $\lambda_{max} \cdot T = 2898$ μm·K (Wien's displacement law). Image reprinted from [115].

If the spectral power of a black body is known, the temperature can be determined from (1) the maximum in the power distribution or (2) total emitted power.

For (1), the temperature is related to the wavelength λ_{max} via Wien's displacement law as

$$T = \frac{C_{Wien}}{\lambda_{max}} \tag{5.2}$$

where C_{Wien} is Wien's constant (2898 μm·K) and λ_{max} is the peak-power position (see Figure 5.1).

For (2), the temperature is related to the area under the $E_b(\lambda)$-curve, which equals $\int_0^\infty E_b d\lambda$ and is known as Stefan-Boltzmann's law:

$$E_b = \sigma T^4 \tag{5.3}$$

where σ is Stefan-Boltzmann constant (5.67051×10^{-8} $Wm^{-2}K^{-4}$).

5.2.1.1 Practical limitations

For a non-ideal object ("grey body"), the amount of the emitted electromagnetic radiation is less than for a black body and depends on properties of the surface (e.g. the material, roughness, etc.). The difference in the emitted power between a grey (E) and black body (E_b) is called the emissivity:

$$\varepsilon(\lambda,T)=\frac{E(\lambda,T)}{E_b(\lambda,T)} \tag{5.4}$$

ε varies between 0 and 1 and is a function of both the wavelength and temperature.

The emissive power of a grey body can be expressed in a modified form of Stefan-Boltzmann's law:

$$E=\varepsilon\sigma T^4 \tag{5.5}$$

In practice, the spectral power of an object is measured in a system with practical limitations. These need to be taken into account for a reliable temperature measurement [114].

Typical limitations are:

1. The medium through which the radian energy is transmitted towards the detector can adsorb a part of the spectrum.
2. The transducer or (IR) detector, to convert the radian energy into electrical energy, is wavelength dependent and has non-linear *E-I* characteristics (offsets, saturation).
3. Amplification / signal processing to make the measurement results in quantification errors of the electrical signal (AD conversion, noise). Furthermore, the time resolution is limited by the integration time. For a steady-state situation, a non-zero integration time is not a problem.

5.2.2 Setup for IR measurements

The setup used for IR temperature measurements is shown in Figure 5.2. It is described in detail elsewhere [31]. It consists of a XEVA IR camera with InGaAs detector having a wavelength response between 0.9-1.7 µm. It is mounted on a PM8 probestation equipped with an IR optical column.

The IR emission is measured for a certain integration time (t_{int}) and is quantified by a 14 bit AD-converter. The latter has a dynamic range of 2^{14}=16384 bits or analog-to-digital units [ADUs]. A schematic representation of the output signal versus light intensity is shown in Figure 5.3. The signals matching the lower (*x_black*) and upper limit (*x_white*) of the AD-converter are chosen such that the IR sensor is operated in its linear regime. The integration time is chosen in accordance to the optical signal by maximizing the measured IR signal without saturation >16384 ADU). For each integration time, a different set of *x_black*, *x_white* and *x_grey* values is used.

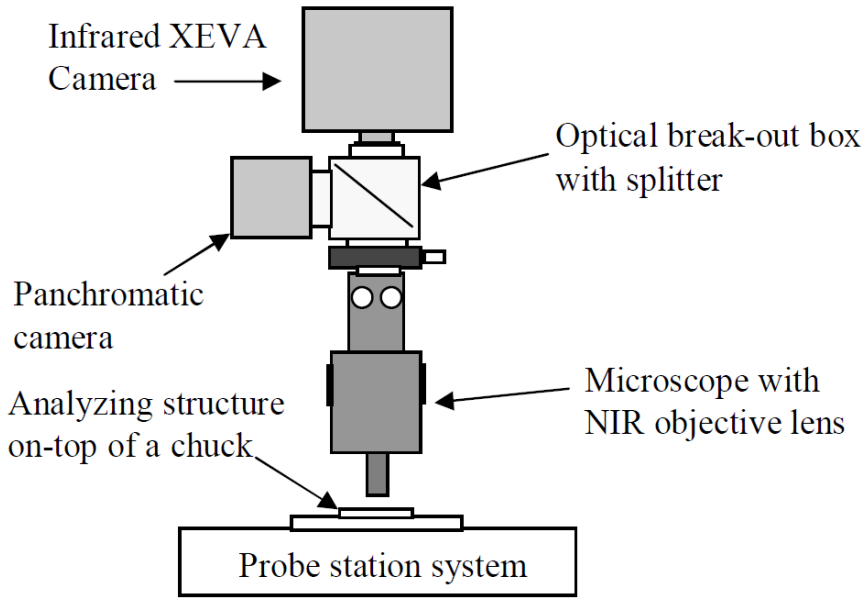


Figure 5.2: Schematic representation of the setup for IR measurements. Image is based on ref [31].

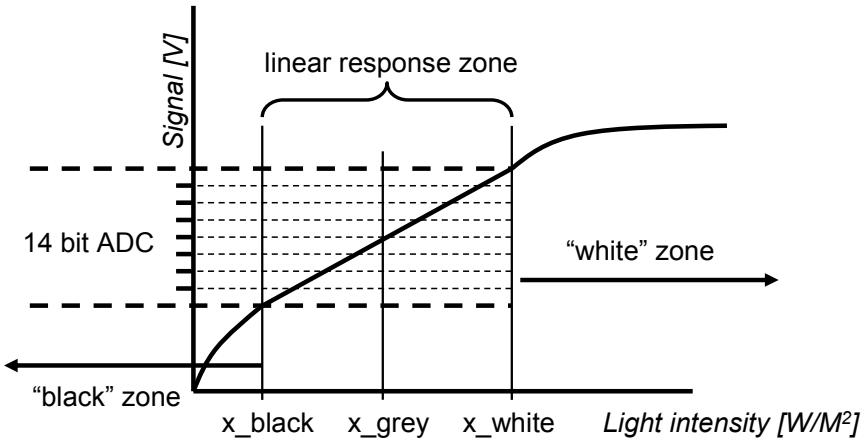


Figure 5.3: Output signal of the IR camera vs the light intensity. x-black and x_white, corresponding to 0 and 2^{14}=16846 ADU, respectively, refer to the lower and upper limits of the output signal and are chosen to match the boundaries of linear regime of the IR sensor. x_grey is the output signal at 50 % and used to adjust the AD-converter.

5.2.2.1 Characterization of the setup for IR measurements

Given the bandwidth of the camera (0.9-1.7 μm) and the temperature range of interest (25-600ºC $\Rightarrow$ λ_{max} = 3.3-9.7 μm), the temperature of SMA hot surfaces cannot be extracted via neither Wien's law (5.2) nor Stefan-Boltzmann law (5.3). However, according to Planck's law the IR light intensity within the bandwidth of the camera is a measure of the temperature: $\int_{0.9}^{1.7} E_b d\lambda$. This does not account for all other non-idealities of the setup (e.g. the adsorption of the optical column, the non-linear response of the IR camera, etc.). These practical limitations of the setup can be quantified and taken into account by measurements on a commercially available microelectronic (reference) hotplate with well established electrical / surface temperature characteristics [116]. This reference hotplate is a conventional microelectronic heater [3, 6] based on an unpassivated platinum thin film that is patterned in a meander shape. The heater is positioned on top of a suspended silicon nitride membrane.

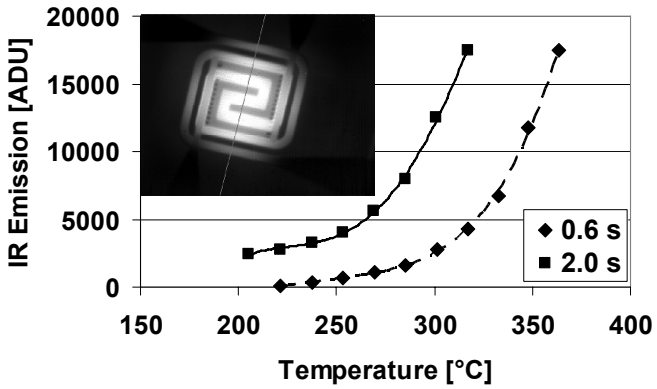


Figure 5.4: Measured IR emission (or intensity) vs the temperature for a commercially available microelectronic hotplate with 0.6 s and 2.0 s integration time. For 2.0s integration, the noise floor is 2400 ADU; data within the noise floor is omitted. Lines are 4th order polynomial fits through the data. The inset shows the IR image of the device in operation. The IR emission is extracted from the centre of the device.

Resembling the SMA, the heater temperature is extracted via the temperature dependence heater resistance. As the heater is situated at the surface, the surface temperature is equal to the heater temperature for the reference device.

In Figure 5.4, the measured IR emission (or intensity) versus the temperature is presented for two integration times. The IR emission is extracted at the centre of the device (see inset). The lines are 4th order polynomial fits through the data: indeed the measured IR emission follows a 4th order dependence on the temperature. Furthermore, it is observed that a temperature range of ~150 °C at maximum can be measured within the dynamic range of the camera for a single integration time. Lower temperatures are not detected, higher temperatures lead to saturation.

In Figure 5.5, the measured IR data are shown versus the temperature together as well as the theoretical curves of Stefan-Boltzmann's law and Planck's law for a blackbody (i.e. $\varepsilon = 1$). Planck's law is integrated over the optical range of the camera, i.e. 0.9-1.7µm. Different slopes are observed for both Stefan-Boltzmann's and Planck's law as well as for both integration

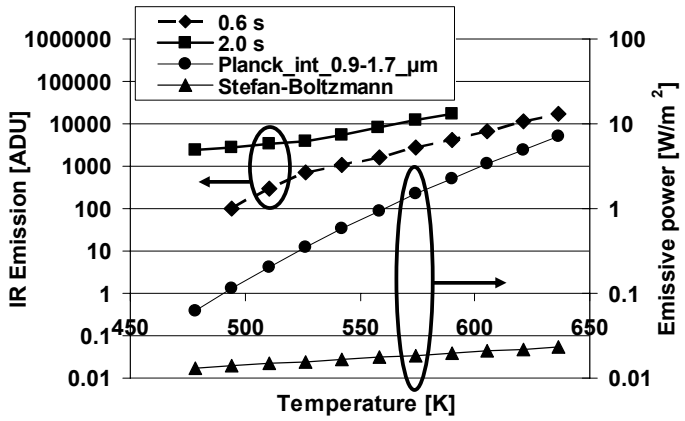


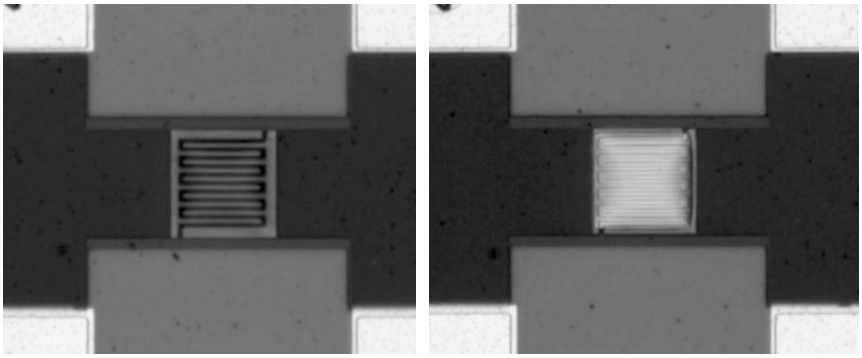
Figure 5.5: Measured IR emission vs temperature data together with calculated emissive power according to Planck's and Stefan-Boltzmann's law with ε=1. For Planck's law, eq (5.1) is integrated over the spectral range of the IR camera (λ = 0.9-1.7 µm).

times. This shows that the experimental data obtained from the IR camera cannot be modelled by simple scaling of neither Stefan-Boltzmann's or Planck's law models, nor by scaling with the ratio of the integration times. This is the result of non-linear components in the optical system.

Thus for each integration time, the IR emission versus temperature characteristic needs to be measured using a reference device to determine the temperature range and the IR emission-temperature relation within that temperature range.

5.2.2.2 Calibration device for SMAs

In order to measure the temperature of SMAs with IR thermometry, a special test structure (calibration device) is fabricated with the same layers and surface properties and hence the same emissivity as SMAs. The calibration device is fabricated in the same fabrication process with the same layer stack on top of the heater (7 nm ALD TiN + 16 nm Al_2O_3 / 100 nm SiO_2) as the SMAs. In the calibration device, the heater is the ALD TiN thin film, which is patterned to a meander shape (see Figure 5.6a). Some devices are covered additionally with a 100 nm thick platinum rectangular disk (Figure 5.6b). The calibration devices have a high Ohmic (~20 kΩ) heater



(a) *(b)*

Figure 5.6: Optical micrographs of a meander-type calibration device without (a) and with platinum disk (b), for calibration of the IR setup for SMAs.

with a TCR of the (flat) ALD TiN film, relatively uniform surface temperature distribution and a large heating area.

In Figure 5.7, temperature versus power curves are shown for a device without and with platinum disk, operated under constant power conditions. The temperature is extracted from the change in heater resistance and the TCR, similar to the procedure for the SMA (see section 4.5.2.1). It is observed that for the device with platinum disk, more power is required to maintain the same heater temperature; this can be attributed to the increased heat-losses to the substrate via the platinum disk.

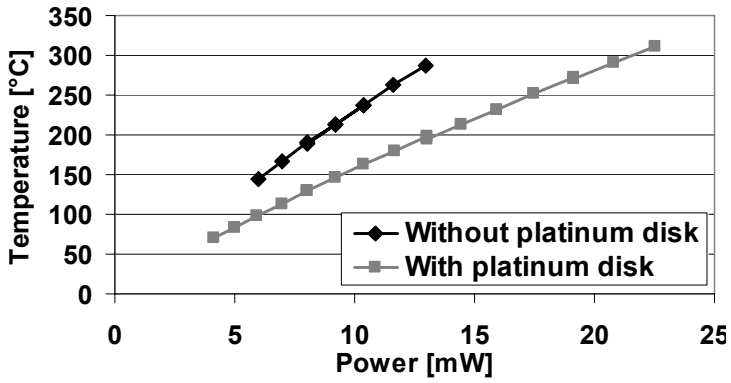
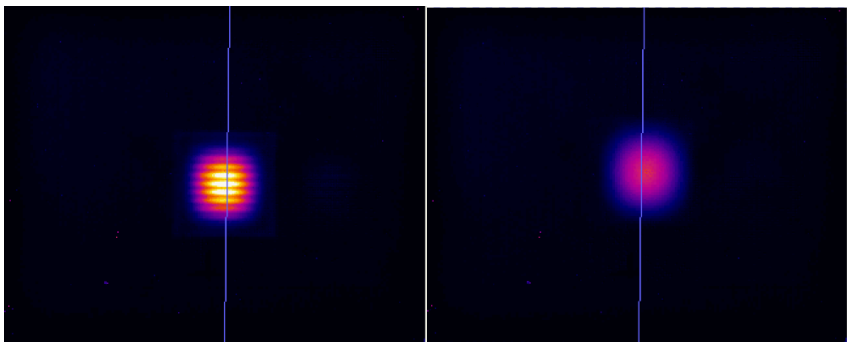


Figure 5.7: Temperature vs power characteristics for a meander-type calibration device without and with platinum disk.

In Figure 5.8, IR images are shown of a calibration device without (Figure 5.8a) and with platinum disk (Figure 5.8b). The camera is operated at the maximum sensitivity with an integration time of 10 s. This is practically speaking the maximum: higher integration times dramatically increase the noise in the image and hence decrease the dynamic range of the camera.

For both devices, the temperature is ~290 ºC, based on the heater resistance. It is observed that the platinum disk emits less IR radiation than the device without the disk; this is because the emissivity of the platinum disk ($\varepsilon_{Pt} \approx 0.1$ at 200 ºC) is lower than that of the device without the platinum disk, which is covered with 16 nm Al_2O_3 and 100 nm SiO_2 ($\varepsilon_{Al2O3} \approx 0.7$ and $\varepsilon_{SiO2} \approx 0.8$ at 200 ºC) [114, 117].

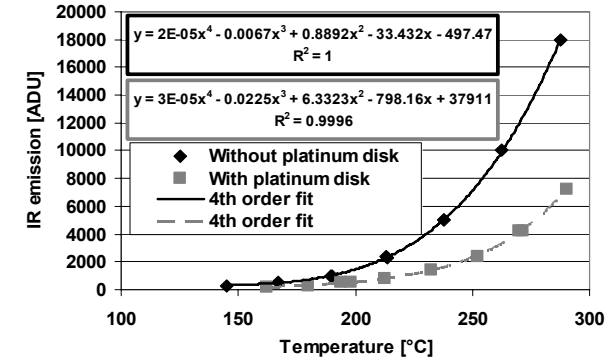
The IR emission is extracted from the centre of the device. Figure 5.9a shows the emission versus the applied power for both the device without and with the platinum disk. For both sets of data, a 4th order polynomial function can be used to interpolate the data. Both curves can be used for calibration of temperature measurements of SMAs, to relate the IR emission to the device temperature.



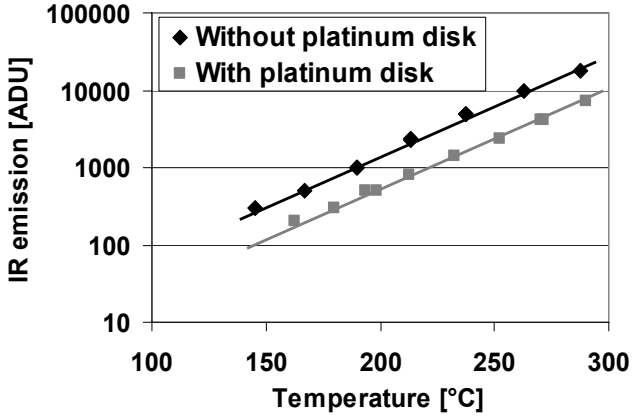
(a) *(b)*

Figure 5.8: IR images of meander-type calibration device without (a) and with platinum disk (b) for calibration of the IR setup. The applied power is 13 mW and 21 mW for the device without and with platinum disk, respectively. The temperature in the centre is ~290 ºC for both devices. The vertical blue line in both images is an artefact of the IR imaging software.

In Figure 5.9b, the data is shown on a logarithmic scale. Lines with identical slopes can be fitted through both sets of data, indicating a constant difference in IR emission of a factor ~2.5 between the devices with and without platinum disk. This indicates the emissivity of the device (see eq. (5.5)) with a platinum disk is a factor of 2.5 lower than that of the device without the disk.



(a)

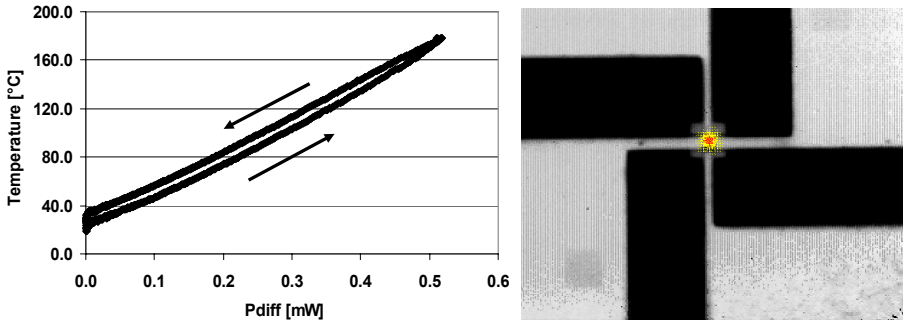


(b)

Figure 5.9: (a) IR emission vs temperature of a meander-type calibration device without and with platinum disk for calibration of the IR setup. A microscope magnification of 10× is used in combination with an integration time of 10 s. Lines are 4th order polynomial fits through the data. (b) Same data on a logarithmic scale. Lines with identical slope are drawn as guide for the reader.

5.2.3 Microlink-based SMAs

In Figure 5.10a, the temperature versus power characteristic is shown for a microlink-based SMA without platinum disk together with the IR microscope image (Figure 5.10b) at a power dissipation in the microlink of 0.5 mW. In this image, the device itself is shown in a grayscale and the IR emission is an overlay in colour. The IR image is measured with the same settings (t_{int}= 10 s, 10× magnification, etc.) as the calibration curve in Figure 5.9. The temperature in the $T(P_{diff})$-plot is extracted from the change in the link resistance and the TCR. IR radiation is detected in the centre of the device, indicating heating in the link area. The extracted IR emission in the centre is 600 ADU which corresponds, according the calibration curve in Figure 5.9, to a temperature of ~175 ºC. Based on the electrical measurement, the link temperature is ~171 ºC. These results indicate that the link temperatures, extracted from electrical and IR measurements, are in very good agreement. It is concluded that the calibration curve shown in Figure 5.9 can be successfully applied to SMAs without a platinum disk.



(a) *(b)*

Figure 5.10: Temperature vs power dissipation in the link (a) for a microlink-based SMA without platinum disk and corresponding IR image (b) at a (constant) power dissipation of 0.5 mW. The image is a composition of the device depicted in a grayscale with the IR emission in colour. The IR emission measured in the centre is 600 ADU which corresponds to a temperature of 175 °C (see Figure 5.9).

5.2.4 Nanolink-based SMAs

Several experiments are carried out on nanolink-based SMAs. As the nanolink is a very small (submicron) source with a low IR emission intensity, it is important to operate the IR imaging system at maximum sensitivity.

The system is at maximum sensitivity with the longest integration time (practically 10 s) in combination with the optimal magnification of the microscope for this IR source. For the microscope, magnifications of 10×, 20× and 50× with special (near) IR transparent (NIR) objectives are available [31]. Assuming that the nanolink is a point source, the system is at maximum sensitivity when all IR emission, produced by the IR source, is projected by the microscope to a single pixel of the camera. The IR camera has a resolution of 256×320 pixels. At magnifications of 10×, 20× and 50×, one pixel corresponds to an observed area of the sample of approximately 1.6^2, 0.79^2 and 0.30^2 μm^2, respectively.

Given the limited spectral range of the camera (λ = 0.9-1.7 μm) and the fact that most of the IR signal is expected around 1.7 μm (i.e. at the right-hand edge of the spectrum, see Figure 5.11) within this bandwidth, the most IR radiation (within the spectral range of the camera) is projected to a single pixel for a magnification of 10×. This shows that a magnification of 10× is the optimal magnification for observing nanolink-based SMAs.

In Figure 5.9, it is shown that the IR emission of a device without platinum disk is a factor ~2.5 higher at the same temperature than that of a device with a platinum disk. For the highest sensitivity, an SMA without platinum disk is used for the IR temperature experiments.

For all the experiments on nanolink-based SMAs without and with platinum disk with link temperatures in the range of 25 – 300 ºC (based on TCR / electrical measurements), no IR emission in the link area is observed. It is concluded that the IR setup is not sensitive enough to detect heating, up to 300 ºC, generated from very small nanolink-based sources.

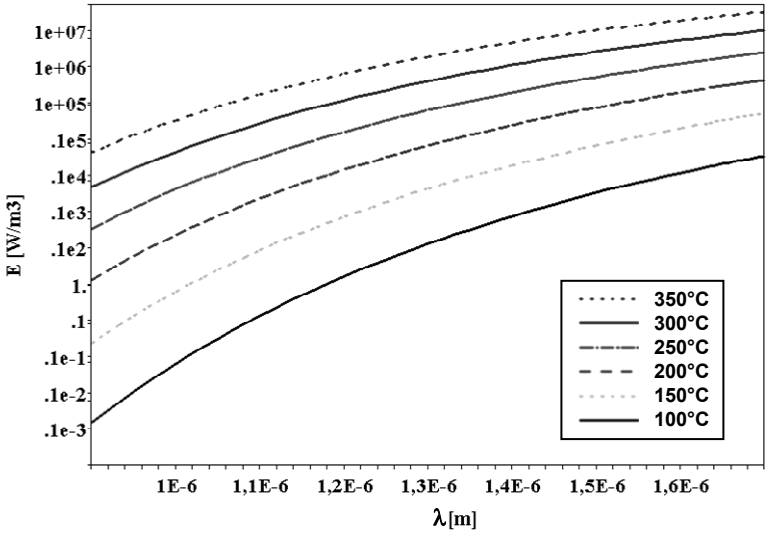


Figure 5.11: Calculated spectral densities (Planck curves) for a black body (ε=1) in the spectral range of the IR camera (λ = 0.9-1.7 µm) for temperatures in the range of 100-350ºC. The spectral power decreases by more than 3 orders of magnitude for wavelengths of 1.7 µm down to 0.9 µm in this temperature range.

5.3 Polymer melting

5.3.1 Introduction, method and metrology

The temperature of a surface can be determined by observing the phase transition of a material that is in contact with the surface, while increasing the temperature. This technique is used for calibration of, for instance, micromechanical probes for temperature measurements [118, 119] or calorimetric experiments [120]. Generally, the glass transition (T_g) or melting temperature (T_m) of polymers (T_m = 36-260 ºC [118, 121]) or metals (T_m > 156 ºC [77]) is used.

The heat (Q in [J]) transferred to a material on top of a heater causes a change in temperature (ΔT in [ºC]) of the material and can be expressed by

$$Q = mc\Delta T \qquad (5.6)$$

where m is the mass [kg] and c is the heat capacity (J/(kgºC)) [122].

For this technique it is assumed that the heat capacity of the heater is large compared to the melting material, which means the thermodynamic behaviour is 'quasi-static'. In other words, the time constants associated with the heat transfer to the melting material are small enough for the melting material to follow the heater temperature during a temperature ramp.

In this work, this method is applied to nanolink-based SMAs using tricosane ($CH_3(CH_2)_{21}CH_3$). Tricosane (> 99.5 %, Sigma Aldrich, 91447) is a paraffin-like polymer with a melting temperature of 47-49 ºC [123]. The devices are characterized using the IR setup described in section 5.2.2; the phase transition (solid to liquid) of the polymer is observed using the IR camera under sample illumination by the microscope light. Both optical (movie) and electrical (*IV*-characteristics) data versus time are recorded simultaneously and later synchronized in time.

5.3.2 Meander-shaped calibration device

Before application to SMAs, the polymer melting method is verified using the calibration device for IR measurements (see section 5.2.2.2), which has a large surface and well-defined temperature-power relation. A tricosane flake with a diameter of approximately 100 µm is placed on top of the device, then a linear voltage sweep is applied from 0 V to the maximum voltage (V_{max}) and back to 0 V. The heater resistance versus time (t) is shown in Figure 5.12 for 3 consecutive experiments. A detailed graph of the temperature versus time near the melting temperature is shown in the insert. From the resistance change and the TCR, the temperature is extracted and shown on the right-hand axis of Figure 5.12. The same TCR (2.7×10^{-4} /ºC) is used for all the 3 curves. Images of the device with the tricosane flake are taken at various moments (see numbers in Figure 5.12) during the experiment, and are shown in Figure 5.13.

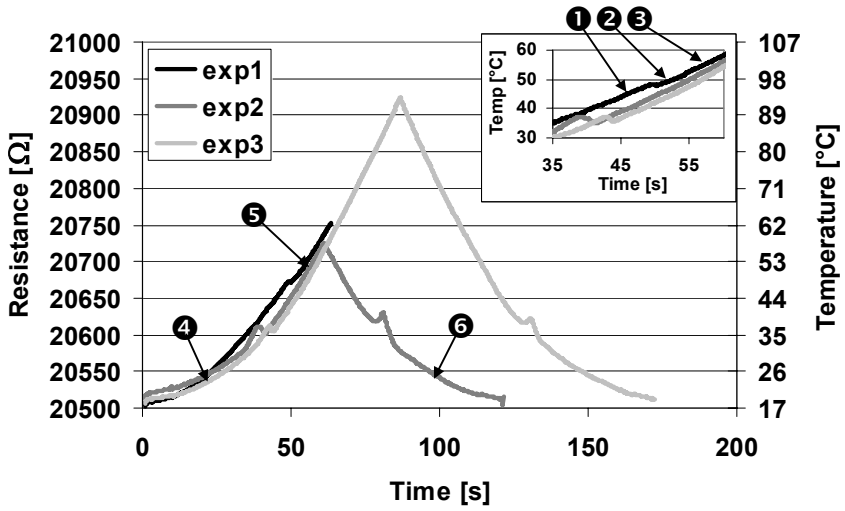


Figure 5.12: Resistance vs time for a meander-shaped heater without platinum disk (calibration device, see Figure 5.6) with a tricosane flake on top for 3 consecutive voltage sweeps ('experiments'). The temperature is extracted from the resistance change using the same TCR (2.7×10^{-4} /ºC) for all 3 curves and shown on the right-hand axis. The inset shows a close-up of the time frame in which melting of the tricosane flake is observed. Numbers correspond to the times for which the images are shown in Figure 5.13.

At the beginning (up to 45 s) of experiment 1 (see point ❶ in Figure 5.12), an opaque flake of tricosane is observed (Figure 5.13a). A voltage ramp with V_{max} = 10 V is applied. After 8 seconds, an increased transparency in the tricosane flake (Figure 5.13b) is observed together with a kink (see point ❷ in Figure 5.12) in the $R(t)$-relation. Within 10 s (see point ❸ in Figure 5.12), the tricosane flake becomes completely transparent and decreases in perimeter indicating the complete phase transition from solid to liquid (Figure 5.13c). The temperature, based on the resistance change and the TCR, (i.e. the electrically measured melting temperature (EMMT)), at which the beginning of the phase transition is observed, is approximately 48 °C. This is in agreement with the melting temperature (T_m) of tricosane. Furthermore, it is observed that it takes ca. 10 s to melt the whole tricosane flake.

In the subsequent experiment 2, a voltage sweep is applied to the heater with V_{max} = 7 V, during which the solid tricosane (see point ❹ in Figure 5.12 and Figure 5.13d) melts again (see point ❺ in Figure 5.12 and Figure 5.13e), and cools down to become again the solid phase (see point ❻ in Figure 5.12 and Figure 5.13f). From the optical data, it is observed that it takes 5 s to melt the tricosane for the second time. A humb in the $R(t)$-curve is observed in Figure 5.12, 10 s before the observation of the phase change with the camera. The same humb is observed during solidification of the tricosane (~75 s). The temperature at which tricosane melting and solidification is observed electrically (the EMMT)), is ca. 36-39 ºC. For the next experiment 3, the same observations are made as for experiment 2, for both the optical

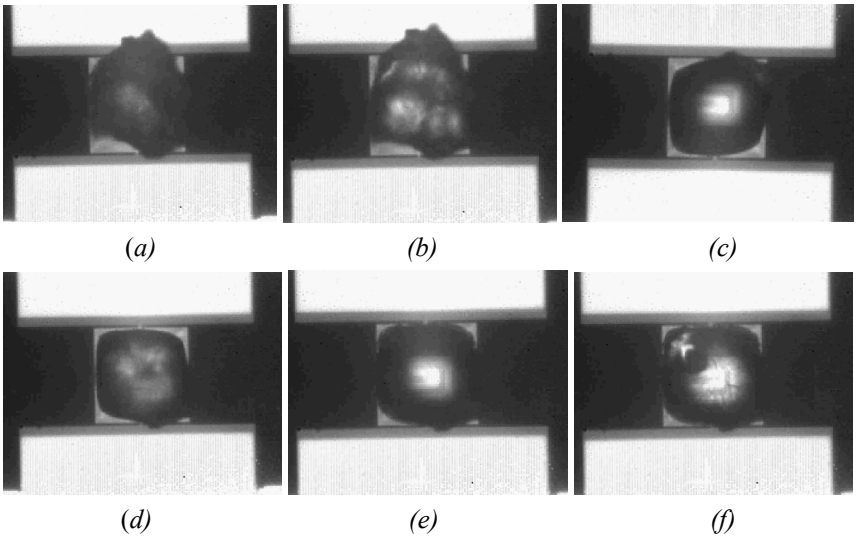


Figure 5.13: Optical micrograph of a meander-shaped heater (calibration device, see Figure 5.6) with a tricosane flake on top at different times (see Figure 5.12) during experiment 1 and 2:
Experiment 1: ❶ solid phase (a), ❷ during melting (b) and ❸ molten tricosane(c).
Experiment 2: ❹ solid phase (d), ❺ molten phase (e) and ❻ solid (f) tricosane.
In (f) tricosane looks less opaque than in (a), but fringes and irregular crystallization are observed in the top left corner indicating the solid phase.

(not shown) and electrical data. This shows that the melting and solidification of the tricosane occurs at the same temperature after the first melt.

The 10 s delay of the optical observation of melting tricosane with respect to the humb in the $R(t)$-curves indicates that the onset of melting can be observed more accurately via the $R(t)$-curve than optically. This is because the liquid tricosane is observed through the opaque (top) part of the tricosane: this is only possible when the majority of the tricosane volume has become liquid. The EMMT of 36-39 ºC is 9-12 ºC lower than the theoretical melting temperature for tricosane (T_m = 47-49 ºC). The shorter tricosane melting time for the 2nd and 3rd sweep is ascribed to the increased contact area and hence better thermal contact of the tricosane with the heater after the first melting. In Figure 5.14, the measured resistance for the three experiments is plotted as a function of the applied power. Here, a similar effect is shown where the melting occurs at a lower power in the 2nd and 3rd experiment: ~1.0 mW compared to 1.6 mW initially.

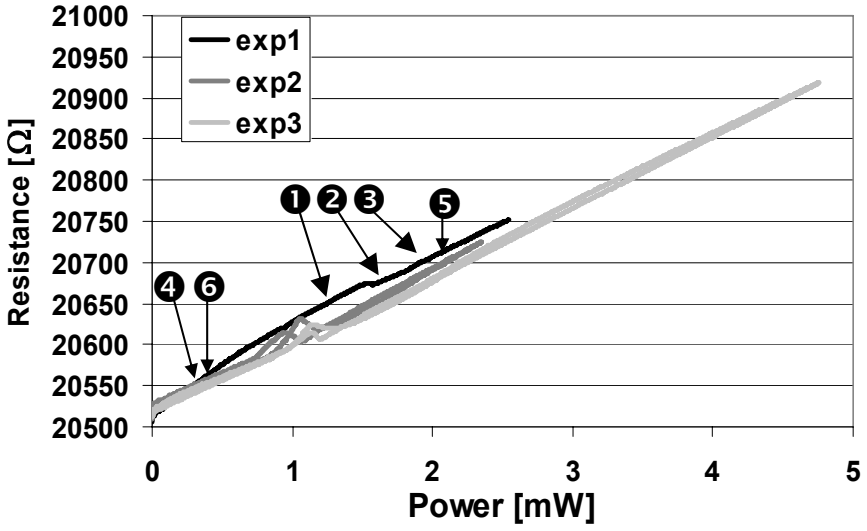


Figure 5.14: Resistance vs power for a meander-shaped heater without platinum disk, corresponding to the experiments as shown in Figure 5.12 and Figure 5.13.

The reasons for the lower EMMT and lower melting power for the 2nd and the 3rd experiment can be twofold. (i) The molten and solidified tricosane on the heater after the first experiment leads to additional heat leakage paths (laterally and towards the substrate). This could result in a different temperature distribution over the heater element. In the resistive temperature measurement the average resistance over the heater element is measured. Although the same heater resistance at room temperature is observed for all 3 experiments (R = 20.5 kΩ at 18 ºC), a different temperature distribution could lead to a different average temperature at elevated temperatures and, in turn, to a different extracted temperature. (ii) After the first melting and cool down a mechanical deformation of the heater and membrane is observed from microscope images. It has been reported that mechanical deformation and stress/strain in metallic thin films affect the TCR [124].

These results show that melting of the tricosane can be observed more sensitive via a change of the heater resistance rather than from optical observations. Moreover, the electrical and thermal behaviour of the device is different after the first melting run. Furthermore, it is shown that it takes 5-15 s to melt the given amount of tricosane at a power of 1.0-1.6 mW. In case that all the heat is transferred to the tricosane flake, melting of a 100×100×10 μm^3 volume of tricosane takes theoretically ~5 s at a power dissipation of 1 mW (see section 5.3.3 for the calculation approach with all material constants). This is within the same order of magnitude as the experimentally determined melting times. Therefore it is concluded that the measured melting times of 5-15 s are physically correct and that the majority of the heat, generated by the heater, is transferred to the tricosane. It is shown that the polymer melting method for temperature measurement can be applied successfully to large area meander type hotplates.

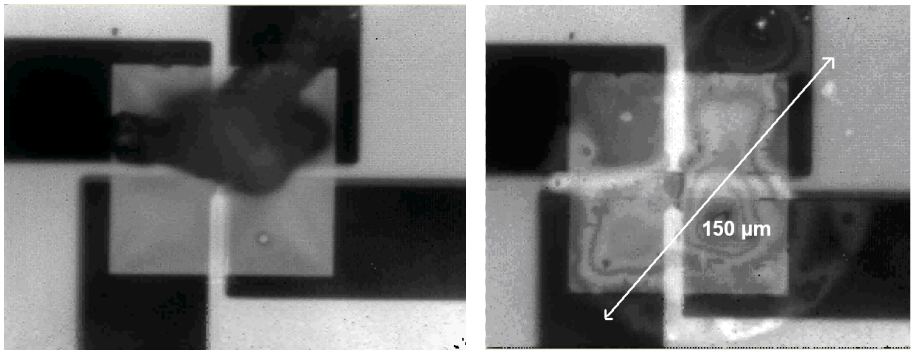
5.3.3 Nanolink-based SMAs

The same polymer melting technique is applied to a 68 MΩ nanolink-based SMA without platinum disk. A flake of approximately 50×100 μm is placed on top of the device, as shown in Figure 5.15a. During application of

a voltage sweep up to V_{max} = 3 V and back to 0 V in 180 s (similar to experiment 3 in Figure 5.12) a maximum power of 4.0 μW is dissipated in the link. At maximum power, the link has, based on a change in resistance and the TCR (-3.3×10^{-3} /ºC), a temperature of ~290 ºC. However, no indication of melting of the tricosane flake is observed from the optical and electrical data.

In order to improve the thermal contact between the tricosane flake and the nanolink, the complete device is heated above the melting temperature of tricosane (60 ºC, using the chuck of the probestation), causing the tricosane to reflow (see Figure 5.15b). Next, two constant voltages are applied to the nanolink-based SMA, resulting in a power dissipation in the nanolink of 5 μW and 14 μW for 20 and 26 min, respectively. During both the experiments, no indications of tricosane melting (electrical via $R(t)$-curves or visual) were observed.

Using eq. (5.6), the heat can be calculated that is needed to heat up the tricosane volume from room temperature (18 ºC) to its melting temperature (48 ºC). Estimating the volume of the tricosane flake, based on microscope



(a) *(b)*

Figure 5.15: Optical micrograph of a nanolink-based SMA without platinum disk with a tricosane flake on top, before (a) and after (b) heating up the whole wafer above the melting temperature of tricosane. After heating up, a cylindrical-shaped volume of tricosane is formed with a diameter of ~150 μm. The (square) membrane area in the centre is 110×110 μm.

observations, to be 100×50×50 μm^3 and with the heat capacity of 772 J/mol·kg [125] and a density of 7.97×10^{-4} kg/cm^3 [126], an energy of 14 mJ is required to heat it up to 48 ºC (see eq. (5.6)). Between the solid and the liquid phase, tricosane has an extra crystalline phase, so two phase transitions are considered [127, 128]: crystalline 1 → crystalline 2 (at 40.5 ºC) and crystalline 2 → liquid (at 47.7 ºC), with the phase transition enthalpies of 21.500 kJ/mol and 52.250 kJ/mol, respectively. Phase change 1 and 2 require energies of 13 and 32 mJ, as calculated for the given amount of tricosane. The total energy required for heating up and melting the tricosane is the sum of these energies, which is (14+13+32=) 59 mJ. In the ideal case, when all the heat, generated by the link, is transferred to the tricosane volume, approximately 21 mJ is generated by the link at a power dissipation of 14 μW in 26 min. This means it should take ~71 min to melt all tricosane. However, this ideal case is not realistic, because heat leaks away to the substrate via for instance the connection electrodes. Therefore, much more time (>> 71 min) is practically required to melt all tricosane. These extremely long times are unrealistic for practical melting experiments.

However, not the complete tricosane volume needs to be heated for electrical detection of a phase change. After melting the tricosane flake (and assuming a constant tricosane volume), a cylindrically-shaped volume of ∅150 μm tricosane is formed (see Figure 5.15b). The height of this cylinder is calculated to be ~14 μm, assuming the volume of tricosane is the same as before melting. Therefore, a smaller volume of tricosane is considered. Given the link is a point-source, a hemispherical volume can be used with a radius of 14 μm, which yields a volume of 2.2 μm^3. Repeating all the calculations above, it can be concluded that melting of this small volume requires a heat of 0.12 mJ. With all the heat generated by the link at a power dissipation of 14 μW and assuming no heat leakage to the substrate, it should take ~9 s to melt this small volume. During 26 min of the experiment, approximately 21 mJ is generated by the link. This means that less than 0.12 mJ / 21 mJ = 0.6 % of the energy generated by the link is transferred to the tricosane volume.

Furthermore, similar to the calibration device, the thermal behaviour of the SMA is completely different after melting the tricosane. An extra path for heat leakage towards the substrate is created via the reflown tricosane, with a large heat capacity compared to the nanolink.

These results show that the polymer melting method, using a $100\times50\times50$ μm^3 volume of tricosane, cannot be used for temperature measurements on nanolink-based SMAs. The power that is generated by the nanolink is too low to melt a small tricosane flake at all or within a reasonable time, and the volume (and hence the thermal capacity) of the tricosane flake is too large for a proper calorimetric experiment with the nanolink as a heater.

5.4 Conclusions

In this chapter, two techniques, infrared (IR) thermometry and polymer melting, are explored for determining the link temperature of SMAs different from the resistive temperature measurement technique.

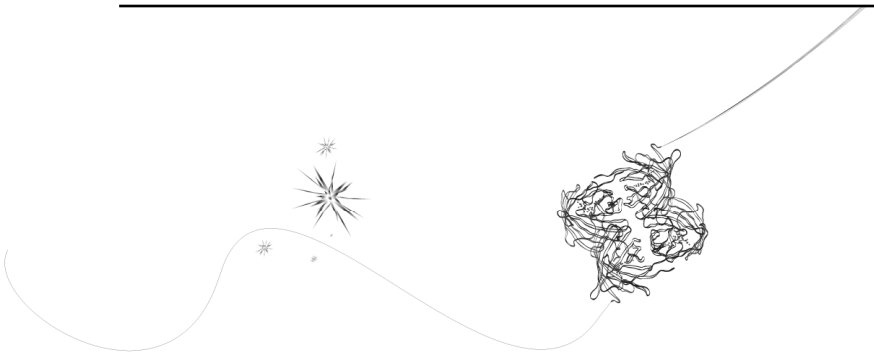
The setup for IR thermometry (λ=0.9-1.7 μm) is characterized using a commercial available microelectronic heater for two integration times. The measured IR emission versus temperature (*E*-*T*)-relation is compared to Planck and Stefan-Boltzmann models. It is shown that the output signal cannot be modelled by simple scaling of neither Stefan-Boltzmann's or Planck's law models, nor by scaling with the ratio of the integration times, but needs to be calibrated with a large area microeletronic heater ('calibration device') having exactly the same layer composition and hence the same emissivity as SMAs. For the setup at maximum sensitivity, the *E*-*I*-relations are obtained for calibration devices with and with platinum disk. The emissivity of the device with platinum disk is a factor 2.5 lower than of the device without platinum disk. Using this calibration, it is shown that the temperatures, extracted from the temperature dependent electrical link resistance and IR measurements, are in excellent agreement for a microlink-based SMA without platinum disk.

For nanolink-based SMAs, no IR emission can be measured for (electrically measured) link temperatures up to 300 ºC as the IR setup used is not sensitive enough.

The polymer melting technique is applied to the same large area calibration device without platinum disk, as used for IR experiments, using a $100\times100\times10$ μm^3 flake of tricosane. The phase transitions can be observed visually via a camera and electrically via a change in heater resistance. The electrical measurement is more sensitive. Furthermore, it is shown that the electrical and thermal behaviour of the device (i.e. a difference in the electrically measured melting temperature) is different after the first melting run. The measured melting times are physically correct, and the majority of the heat, generated by the heater, is transferred to the tricosane. The thermal capacity of the tricosane flake is in the same order of magnitude as that of the large area heater. It is shown that the polymer melting method for temperature measurement can be applied successfully to large area meander type hotplates.

The method cannot be used for temperature measurements on nanolink-based SMAs using a $100\times50\times50$ μm^3 volume of tricosane. The energy produced by the nanolink is too low to melt a small tricosane volume at all within a reasonable time, and the volume (and hence thermal capacity) of the tricosane flake is too large for a proper calorimetric experiment with the nanolink as a heater.

6 The process integration of ALD TiN in SMAs



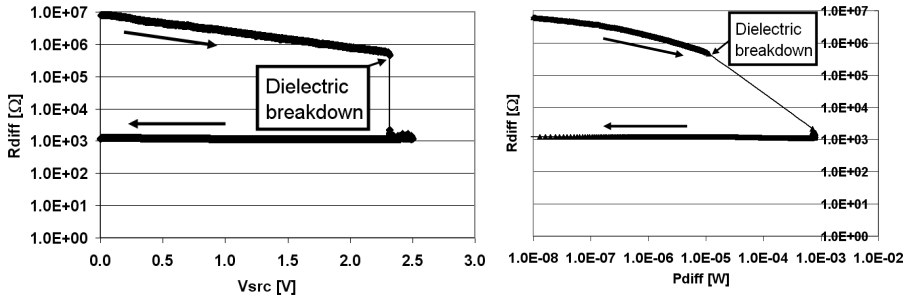
6.1 Outline

In this chapter, the electrical behaviour of SMAs is discussed in more detail. For some SMAs, the ICPECVD silicon oxide (SiO_2) layer between the top and bottom electrode sometimes loses its insulating properties (dielectric breakdown) and exhibits high leakage currents for low electric fields. Given the intrinsic properties of the materials used, the electric field across the SiO_2 layer at which dielectric breakdown occurs is unexpectedly low.

In this chapter, this issue is investigated in more detail. The specific combination of a patterned sputtered TiN bottom electrode in combination with the presence of an ALD TiN layer in the top electrode is demonstrated to be the cause for the observed electrical behaviour. Based on HRSEM and FIB analysis, it is shown that the dielectric breakdown and the high leakage currents are related to the process integration of ALD TiN thin films.

6.2 Electrical breakdown of nanolink-based SMAs

In Figure 6.1a, the link resistance (R_{diff}) versus the applied voltage (V_{src}) is shown for an 8 MΩ nanolink-based SMA, for a voltage sweep from 0 to 2.5 V and back. Starting from 0 V, for voltages lower than 2.3 V, a decrease in resistance is observed, consistent with self heating of the nanolink with a negative TCR (see section 4.5.3.2, Figure 4.18a). At V_{src} = 2.3 V, a sudden



(a) *(b)*

Figure 6.1: R_{diff} vs V_{src} (a) R_{diff} vs P_{diff} (b) for an 8 MΩ nanolink-based SMA during dielectric breakdown of the SiO_2 layer between the top and bottom electrode.

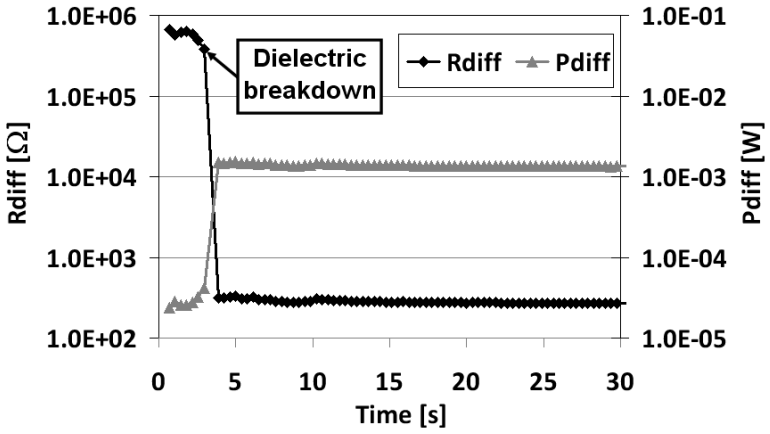
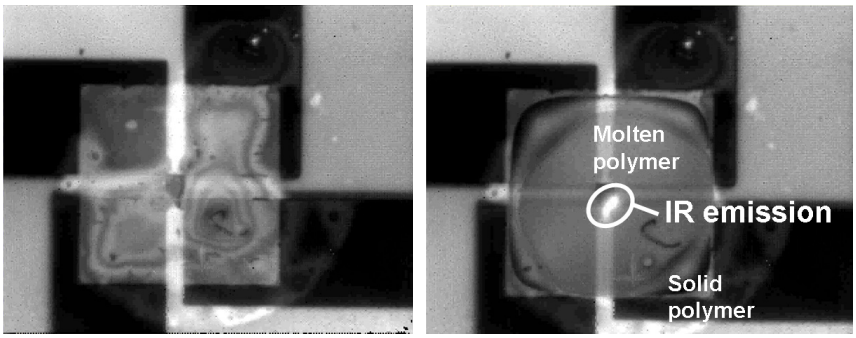


Figure 6.2: R_{diff} and P_{diff} for a nanolink-based SMA during application of a constant voltage of 4.1 V. Dielectric breakdown of SiO_2 occurs at 4 s.

decrease in the link resistance is observed of more than two orders of magnitude. Continuing the voltage sweep up to 2.5V and back to 0 V, the link resistance remains constant at a value of approximately 1 kΩ. As a result of the resistance decrease at 2.3 V, the power dissipation (P_{diff}) in the nanolink increases with a factor 65 from 11 μW to 710 μW at 2.3 V (see Figure 6.1b).

A similar resistance change is observed when a constant voltage is applied to an 68 MΩ nanolink-based SMA (Figure 6.3a) that is coated with a thin polymer layer (tricosane, see section 5.3.3). In Figure 6.2, the resistance and the power dissipation of the nanolink are shown versus the time during application of a constant voltage of 4.1 V. After 4 seconds, the link resistance changes by 3 orders of magnitude to a value of ~280 Ω, while the power dissipation increases by a factor of 58. From this moment, a strong IR emission is observed as well as melting of the tricosane in the central area of the device (Figure 6.3b). Both observations indicate heating of the device. Given the IR emission is exceeding the range of the camera (saturation) and the very low integration time of the camera (3 ms instead of 10 s for the calibration curve in section 5.2.2.2), the temperature is >> 250 ºC. The IR radiation is emitted from the lower-right corner of the square where both electrodes cross each other (Figure 6.3b).



(a) *(b)*

Figure 6.3: IR image (a) of a nanolink-based SMA (illuminated by the microscope light) with a molten polymer (tricosane) on top. Same device after the drop in R_{diff} and the increase in P_{diff} (b). IR light is emitted from the edge of the square where both the electrodes cross each other. Furthermore, molten tricosane is observed in the central area. Both the IR emission and the molten tricosane are the result of heating the device.

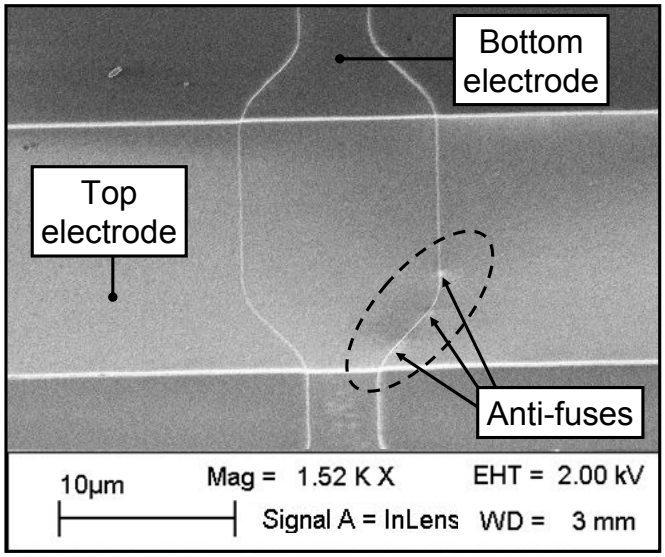


Figure 6.4: HRSEM image of the nanolink-based SMA, shown in Figure 6.2 after resistance change at 4 s and in Figure 6.3. The features in the IR emission area are the result of a difference in conductivity of the electron beam of the HRSEM, these are conductive parts in the SiO_2 (anti-fuses) after breakdown of the SiO_2 layer.

The sudden drop in resistance is caused by the dielectric breakdown of the SiO_2 layer between the top and bottom electrode. SiO_2 loses its insulating properties when a certain breakfield field (E_{BD}) across the oxide is reached [88], as in Figure 6.1a. Oxide breakdown can also be characterized in terms of time-to-breakdown (t_{BD}) when constant voltage stress (CVS) is applied at a voltage close to the breakdown voltage [67], as in Figure 6.2. After breakdown, a low-ohmic conductive path is formed in the SiO_2, which is called an anti-fuse (see section 1.2.2).

A HRSEM image of the central area of the SMA where top and bottom electrodes cross each other, is shown in Figure 6.4. In the area where previously IR radiation is emitted (Figure 6.3b), three features are observed. These features are anti-fuses. Although they are very small (sub 10-100 nm [1]), they can be observed as they give rise to a variation in surface conductivity, and hence a contrast variation of the observed layer stack in the HRSEM. The anti-fuses are present at different locations than the nanolink, which indicates dielectric breakdown of the SiO_2 layer between the top and bottom electrode, parallel to the nanolink.

The anti-fuse behaviour can be described in an electrical model by a resistor (R_{SiO2}) parallel to the link resistor (i.e. $R_{link} = R_{cyl} + R_{cont}$, see Figure 4.4). This is shown in Figure 6.5. The anti-fuse resistance is orders of magnitude smaller than R_{link}, therefore dominating the electrical behaviour of the device.

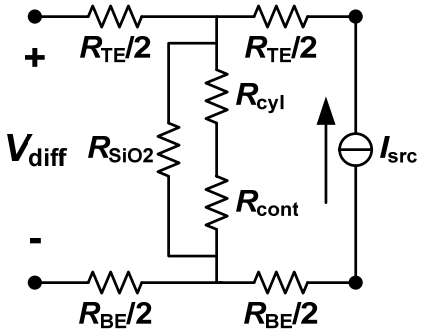


Figure 6.5: Electrical model of the SMA after SiO_2 breakdown and formation of the anti-fuse ("R_{SiO2}") parallel to the nanolink resistance (R_{cyl} in series with R_{cont}, see Figure 4.4b).

Electrical breakdown occurs for a certain E_{BD} across the oxide. For the first device, shown in the previous section (Figure 6.1), E_{BD} is calculated as the voltage at which dielectric breakdown occurs, divided by the oxide thickness (t_{ox}). In a first approximation, the oxide thickness is ~100 nm, which yields a breakdown field 0.25 MV/cm for a breakdown voltage of 2.5 V. This is an order of magnitude lower than the breakdown field of ~6-11 MV/cm for the same high quality ICPECVD SiO_2 layer, measured by Boogaard *et al.* [63].

In the SMA design, the ICPECVD SiO_2 layer is deposited on top of a 100 nm thick sputtered TiN bottom electrode. Because of the non-ideal step coverage of the ICPECVD process, the SiO_2 layer can be thinner near the edge of the TiN bottom electrode. In Figure 6.6, a FIB cross-section of such a TiN layer is shown, covered by a (different) 50 nm PECVD SiO_2 layer. As a result of a non-ideal step coverage, the SiO_2 thickness at the TiN sidewall is lower (by a factor two) than the SiO_2 layer thickness on the flat surface.

For SMAs, this would mean a two times higher E_{BD}; i.e. 0.5 MV/cm. This is still much lower than the expected breakdown field (~6-11 MV/cm) [63].

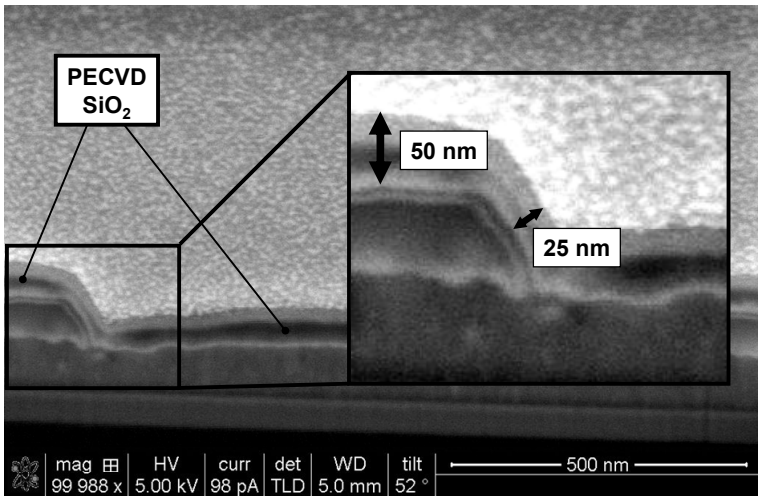


Figure 6.6: FIB cross-section showing the step coverage of a 50 nm PECVD SiO_2 layer. From the measurements, a step coverage of 25 nm / 50 nm = 0.5 is extracted.

6.2.1 Comparison of two integrated plasma-SiO_2 layers

The quality of the SiO_2 layer, integrated in SMAs, is investigated using SMAs without a conductive link as test structures (see inset in Figure 6.8a). In this work, a 100 nm thick state-of-the-art low temperature (150 ºC) ICPECVD silicon oxide layer [63] is used as dielectric in SMAs. The oxide integrity is compared with another ('standard') SiO_2 layer, deposited from SiH_4 and N_2O at 300 ºC in a Plasmalab80plus PECVD system by Oxford Instruments. This layer is referred to as "PECVD" SiO_2.

Both oxide layers ("ICPECVD" and "PECVD" SiO_2) are characterized using the same test structures (SMAs without a conductive link). A (positive) voltage ramp (V_{src}) is applied to two adjacent electrodes of the SMA, while measuring the current (I_{src}) as shown previously in section 4.5.1, Figure 4.10). The *IV*-behaviour is quantified in terms of the E_{BD} and the sub-breakdown leakage current (I_{leak}). E_{BD} is defined here as the electric field at which the current steeply surpasses a level of 10^{-4} A and I_{leak} as the current at an electric field of 0.1 MV/cm. The standard deviation (1σ) is used to quantify the spread of the average E_{BD}-values.

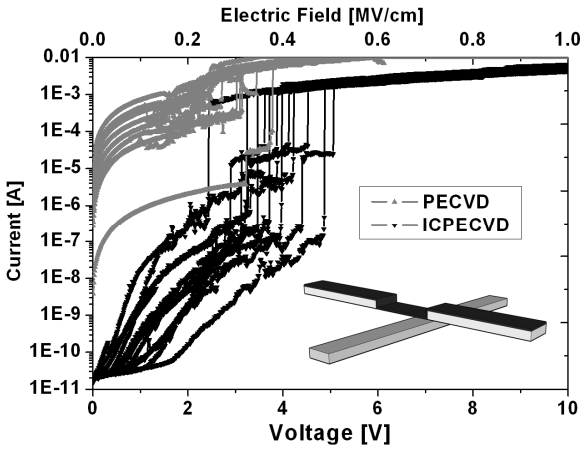


Figure 6.7: Current vs applied voltage characteristics (a) for a PECVD and ICPECVD SiO_2 layer, measured using SMAs without a conductive link as test structure (inset shows a 3D impression of the device). The corresponding electrical field is calculated as the applied voltage divided by the SiO_2 thickness (100 nm for both layers) and shown on the top-axis.

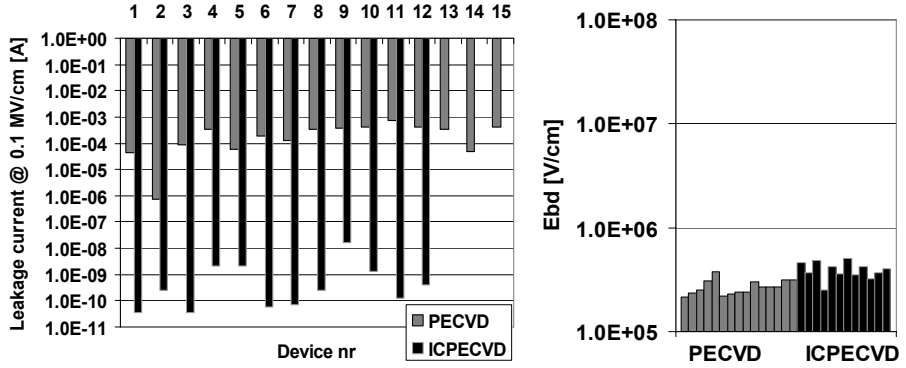


Figure 6.8: Leakage currents at an electric field of 0.1 MV/cm (a) and histogram of the breakdown field (b) corresponding to Figure 6.7; E_{BD} is extracted at the steep current increase in the 10^{-4} A range.

In Figure 6.8, two sets of *IV*-characteristics are shown for both types of the oxide layers. The electric field (E) is calculated as the applied voltage divided by the oxide thickness (~100 nm for both types of layers) and it is shown on the top-axis. This approximation is valid as long as the link resistance >> the connection electrode resistance which is the case for the pre-breakdown regime.

For both types of oxides, I_{leak} is shown in Figure 6.8a.

Average I_{leak}-values of 2.6 ± 2.0×10^{-4} A and 1.9 ± 4.6×10^{-9} A are extracted for the PECVD and ICPECVD layers, respectively. Although the average I_{leak}-value of ICPECVD oxide is 5 orders of magnitude lower than that of the PECVD layer, the corresponding current densities of both layers (~10^{3} and ~10^{-6} A/cm^2, respectively) are still high in absolute terms, compared to a similar high quality ICPECVD SiO_2 layer of the same thickness, measured with a different type of test structure with the same top contact area [39, 63].

Furthermore, E_{BD} is extracted from the *IV*-characteristics and shown in Figure 6.8b. For PECVD and ICPECVD layers, average E_{bd} values of 0.27 ± 0.05 MV and 0.39 ± 0.07 MV are extracted, respectively. Compared to nanolink-based SMAs on a suspended SiRN membrane, having the same ICPECVD SiO_2 layer, (shown in section 6.2 and measured with the same

metrology), E_{BD} (0.39 MV/cm) is higher by a factor of 1.5 for the SMA without link (0.25 MV/cm), but still very low compared to that of a high quality ICPECVD SiO_2 layer (6-11 MV/cm [63]). The difference is most likely due to self-heating of the SMA on a membrane, as E_{bd} decreases at elevated temperatures [8].

These results show both types of plasma-SiO_2 layers exhibit high I_{leak}- and low E_{bd}-values, when integrated in SMAs without a conductive link. Furthermore, it is shown that high I_{leak}- and low E_{BD}-values are correlated.

6.2.2 Device dimensions

In order to find the root-cause of high I_{leak}- and low E_{BD}-values in SMAs, the relation between I_{leak} and the device dimensions is investigated in this section. In the SMA without a conductive link, current can leak between the top and bottom electrode through the SiO_2 layer via the central area of the device, and via the edge where both electrodes cross. Therefore, I_{leak} may scale with the central area (A) or with the perimeter or width (w) of the SMA. The former may indicate that the leakage currents are related to intrinsic properties of the SiO_2 layer, latter could point to the possibility that leaking is through the edge of the bottom electrode (i.e. where the SiO_2 layer is thinner due to the step coverage of the SiO_2 layer over the bottom electrode).

Three sets of SMAs without a conductive link with a 100 nm PECVD oxide layer (see inset Figure 6.8a), are characterized, having w-values of approximately 3, 5 and 10 μm and corresponding areas of approximately 20, 40 and 140 μm^2, respectively. In total, 8 devices of each size are characterized. For the data analysis, w and A are measured by optical microscope measurements for each device. IV-characteristics are measured for voltages up to 50 mV and the leakage current at 50 mV is extracted. Based on the (linear) pre-breakdown IV-characteristics for the PECVD SiO_2 layer, as shown in Figure 6.8a, the current, extracted at 50 mV, is a good indication of I_{leak} (which is defined as the current at 1 V or E = 0.1 MV/cm).

In Figure 6.9a, the leakage current at 50 mV is shown for all devices versus the device width (Figure 6.9a) and the area (Figure 6.9b). No clear

relation between the leakage current at 50 mV and w or A is observed. The average value is ~2.5 ± 0.4×10^{-5} A at 50 mV (which corresponds to I_{leak}=5×10^{-4} A at an electric field of 0.1 MV/cm). This is in accordance with the average I_{leak}-value, extracted from a similar PECVD SiO_2 layer (see Figure 6.9b).

To verify whether there is a correlation between I_{leak} and the device width and area, I_{leak} is normalized to w and A (not shown). The same trend is observed between I_{leak}/W and I_{leak}/A versus w and A, respectively.

This indicates that the leakage current of the PECVD SiO_2 layer at 50 mV (and hence I_{leak} at E= 0.1 MV/cm) does not scale with w or A.

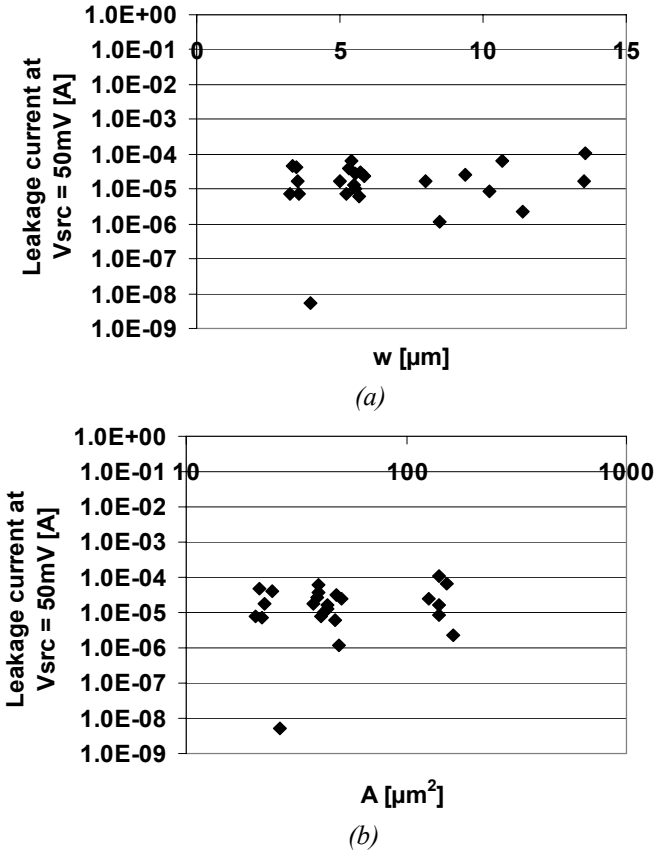


Figure 6.9: Leakage currents at 50 mV for SMAs without a conductive link with various dimensions vs the device width "w"(a) and area "A"(b).

These experiments indicate that the high I_{leak}-values, in SMAs with a high quality ICPECVD SiO_2 layer, do not scale with the width or area of SMA devices. This indicates that leakage is possibly due to random local defects with a low density, otherwise leakage would have scaled with w or A.

6.3 MIS-capacitors with ICPECVD SiO_2

In order to find out more about the root-cause of low breakdown fields and high leakage currents in the SiO_2 layer of SMAs, the intrinsic oxide quality is tested using standard metal-insulator-silicon (MIS) capacitors for the (high quality) ICPECVD SiO_2 layer. MIS-capacitors are used as standard test structure for SiO_2 characterization in the semiconductor industry [67, 88].

MIS-capacitors are fabricated by defining 40×40 μm aluminium squares on an *n*-type silicon substrate that is coated with 54 nm of ICPECVD SiO_2. At the backside of the wafer, 1 μm aluminium is deposited (after removing the native oxide in 1 % HF) and followed by a post metallization anneal in wet nitrogen at 400 ºC for 5 min. More process details are to be found in [63].

The oxide quality of the ICPECVD SiO_2 layer is characterized in terms of E_{BD} and I_{leak}. By applying a positive voltage sweep to the aluminium top contact, electrons in the silicon are attracted to the Si/SiO_2 interface, which are the majority carriers in *n*-type silicon. This means that the MIS-capacitor is operated in accumulation, which implies that the electric field over the oxide can be approximated as the applied voltage divided by oxide thickness [88]. The electric field is shown on the top-axis in Figure 6.10a. In this approximation, the flatband voltage (1-2V for these samples [63]) is neglected as it not significantly affects the breakdown voltage (50-65 V).

In Figure 6.10a, a collection of *IV*-characteristics is shown for these MIS-capacitors. No significant sub-breakdown leakage currents are observed for fields < 6 MV/cm; the measured current at an electric field of 0.1 MV/cm is 0.7×10^{-11} A for all devices, which is equal to the lower measurement limit of the measurement setup. This indicates $I_{leak} \leq 0.7\times10^{-11}$ A. The breakdown field is extracted from all the curves and shown in Figure 6.10b.

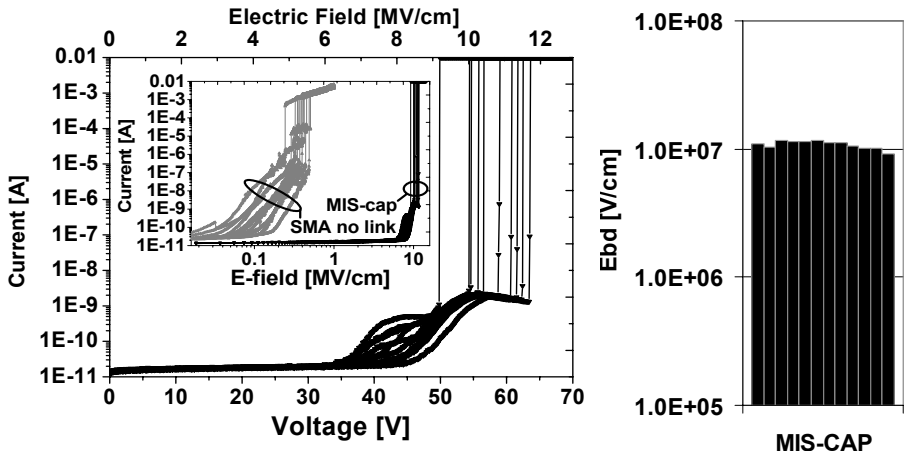


Figure 6.10: Current vs applied voltage characteristics (a) for a 54 nm ICPECVD SiO_2 layer, measured with a standard Metal-Insulator-Silicon (MIS) capacitor as a test structure. The corresponding electric field is shown on the top-axis and the extracted breakdown field in (b). The inset in (a) shows the same data together with I(E)-characteristics of the same ICPECVD oxide, measured using an SMA without a conductive link (see inset Figure 6.7a)

An average E_{BD}-value of 10.8 ± 0.7 MV/cm is observed, which is in accordance the E_{BD}-value (6-11 MV/cm), extracted by Boogaard *et al.* from similar ICPECVD SiO_2 layers [63]. E_{BD} is more than an order of magnitude higher and I_{leak} is almost two orders of magnitude lower, compared to SMAs without a conductive link (see section 6.2.1, the inset of Figure 6.10a).

These results show that the intrinsic quality of the low temperature (150 ºC) ICPECVD SiO_2 layers is high, and it is not the root-cause of the low E_{BD}- and high I_{leak}-values that are observed when the same SiO_2 layer is integrated into the SMAs.

6.4 MIS- and MIM-capacitors with ICPECVD SiO_2

6.4.1 Introduction

In the previous section it is shown that the breakdown field and leakage currents of the ICPECVD SiO_2 layer differ by orders of magnitude, when integrated in SMAs without a conductive link or in MIS-capacitors.

In order to study the quality of the integrated oxide in SMAs systematically, a set of four test structures is fabricated. This set of four test structures contains all four combinations of the two major differences between the previously described SMAs without a conductive link and the MIS-capacitors. These differences are in (1) the presence of an ALD TiN layer in the top electrode and (2) the non-flat topography of the bottom electrode.

The set of four test structures is shown in Figure 6.11. First of all, for the standard MIS-capacitor ("MIS-1", Figure 6.11a), an 8 nm ALD TiN layer is added between the SiO_2 and aluminum layers ("MIS-2", Figure 6.11b). Secondly, SMAs without a conductive link are used, which are referred here to as Metal-Insulator-Metal (MIM) capacitors. Starting with a MIM-capacitor with a sputtered TiN top electrode only ("MIM-1", Figure 6.11c), an 8 nm ALD TiN layer is added, overlapping the top electrode ("MIM-2", Figure 6.11d).

6.4.2 Fabrication

Starting from the MIS-1-capacitor with a 54 nm ICPECVD SiO_2 layer and a flat (silicon) bottom electrode (see section 6.2.2), the MIS-2-capacitor is fabricated by first removing the aluminium layer from the MIS-1-capacitor, from the front and backside of the wafer, using standard wet-chemical aluminum etching. Next, 8 nm ALD TiN is deposited (see section 2.2.3.2), followed by the sputter deposition of 1 μm aluminum. After patterning the aluminum and TiN layers (see section 4.3.1) with a single mask, 1 μm aluminum is deposited on the backside of the wafer, after removing the native oxide in 1 % HF.

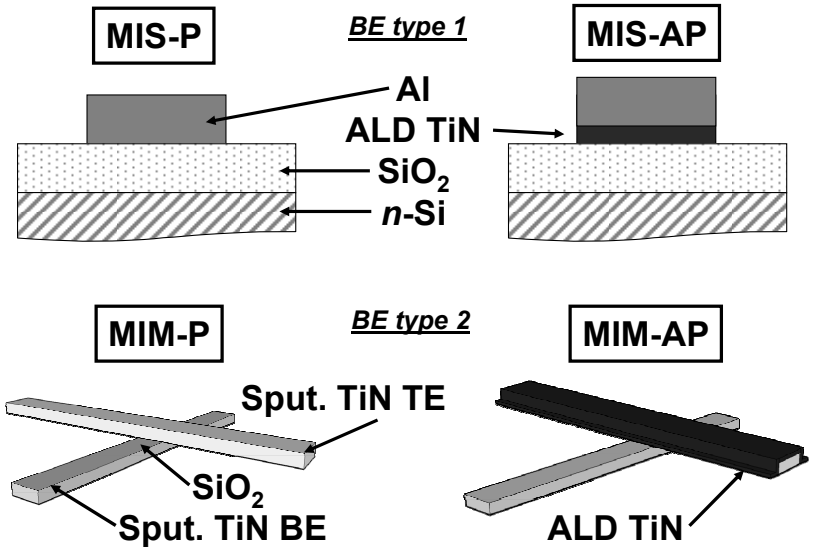


Figure 6.11: Schematic representation of MIS-capacitors with flat bottom electrodes (BEs)(cross-section) and MIM-capacitors (3D) with patterned bottom electrode and various top electrode (TEs): MIS-1 with PVD top electrode, MIS-2 with ALD + PVD top electrode, MIM-1 with PVD top electrode and MIM-2 PVD + ALD top electrode.

MIM-1-capacitors, with a patterned 100 nm sputtered (PVD) TiN bottom electrode and containing a 100 nm ICPECVD SiO_2 layer, are fabricated in the standard SMA fabrication process (described in section 4.3.1). The PVD TiN top electrode is patterned as a continuous line crossing the bottom electrode, in contrast to the discontinuous one of SMAs with a link. For MIM-2-capacitors, an 8 nm ALD TiN layer is added to the top electrode (with the passivation layers, patterned and processed in an identical manner to SMAs, up to including the aluminum contact pad formation). Subsequently, exactly the same devices are measured again (i.e. pre/post ALD of TiN).

6.4.3 Measurements

For all four sets of devices, a positive voltage sweep is applied. The leakage currents (I_{leak}) at an electric field of 0.1 MV/cm are extracted. Cummulative fractions of these currents are shown in Figure 6.12 for 12-16

devices of each test structure design. It is observed that I_{leak} is identical (~0.7 $\times 10^{-11}$ A, the lower measurement limit of the setup) for MIS-1- and MIS-2-capacitors (Figure 6.11a and Figure 6.11b, respectively, both having a flat silicon bottom electrode). This shows that the SiO_2 layer is free from intrinsic structural defects (like pinholes) that increase the I_{leak} significantly.

For MIM-1-capacitors (Figure 6.11c, with PVD top electrode), the I_{leak} is reasonably low at a value of ~7.0×10^{-11} A for all devices, (this is one order of magnitude higher than for MIS-capacitors, but still very low compared to I_{leak} in SMAs without a conductive link (Figure 6.8b). For MIM-2-capacitors (Figure 6.11d, PVD + ALD top electrode), 6 out of 16 device show leakage currents that are significantly larger than 1×10^{-9} A.

For one of these MIM-2-capacitors, *I(E)*-characteristics are shown in Figure 6.13. The leakage current at an electric field of 0.1 MV/cm increases by more than 5 orders of magnitude as a result of the additional ALD TiN deposition. This is similar to the high leakage currents observed in SMAs without a conductive link (see section 6.2).

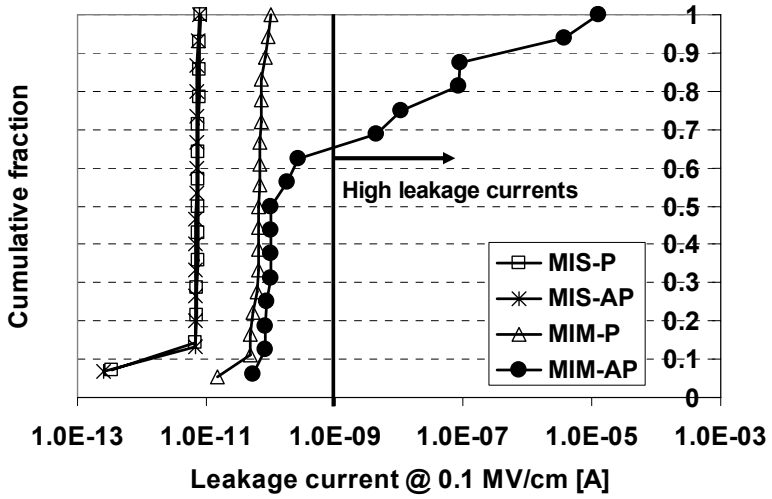


Figure 6.12: Leakage currents at an electric field of 0.1 MV/cm (I_{leak}) for MIS capacitors (flat bottom electrode) with PVD (MIS-1, (a)) and ALD + PVD (MIS-2, (b)) top electrodes and for MIM-capacitors (with patterned sputtered bottom electrode) with PVD (MIM-1, (c)) and PVD + ALD (MIM-2, (d)) top electrodes.

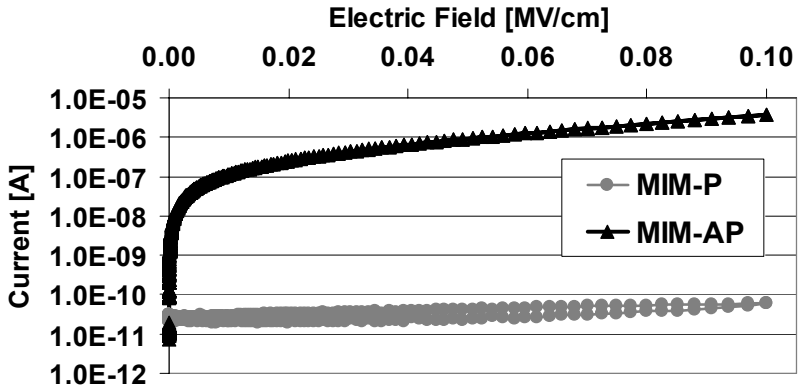


Figure 6.13: I(E)-characteristics for a MIM-1-capacitor with PVD TiN top electrode and for the same device after the deposition of an additional ALD TiN layer (MIM-2-capacitor).

These experiments show that the combination of a pattered sputtered TiN bottom electrode and an ALD TiN layer in the top electrode (MIM-2-capacitors) result in high leakage currents for a significant fraction of the device tested (6/16). This combination is used in our SMAs.

6.5 SEM/FIB analysis

In order to study the root-cause of the high leakage current of MIM-2-capacitors (i.e. basically an SMA without a conductive link), the combination of a TiN bottom electrode and an ALD TiN top electrode in more detail by means of the HRSEM for SMAs.

In Figure 6.14, the top-view of the centre of a nanolink-based SMA is shown, at the position where the top and bottom electrodes cross each other. The sputtered TiN bottom electrode exhibits a rough edge. In addition, a cross-section is made with the FIB at the position where top and bottom electrodes cross each other. A HRSEM micrograph of the cross-section is shown in Figure 6.15. First of all, the rough edge of the bottom electrode is observed. The silicon oxide layer and the ALD TiN layer (with ALD Al_2O_3 and SiO_2 passivation layers) perfectly follow this rough surface of the bottom electrode. Furthermore, particles are present in the rough TiN layer edge and in the capping SiO_2 layer. These particles are also observed in the area where the TiN layer is etched away during formation of the bottom

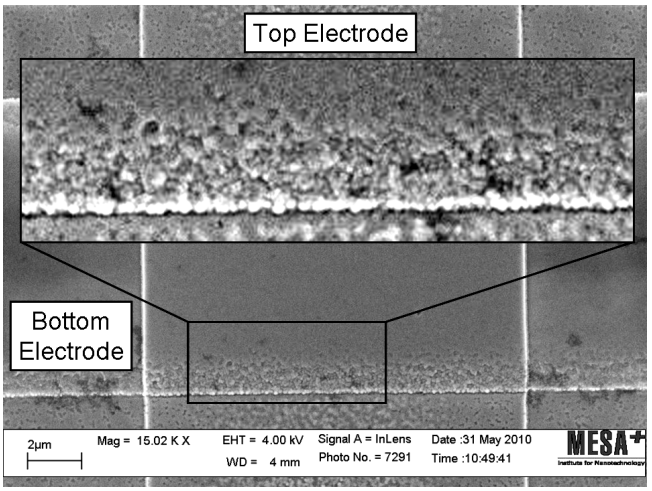


Figure 6.14: (a) Topview HRSEM image (a) of the nanolink-based SMA showing the centre where the bottom (horizontal) and top electrodes (vertical) cross each other. A rough edge of the TiN bottom electrode is observed.

electrode; they result in a rough surface of the top electrode (the left-hand side of the image).

The particles near the edge of the rough bottom TiN electrode lead to structural defects in the SiO_2 layer. These defects become part of the electrical circuit as they are filled with the ALD TiN due to the nearly 100 % step coverage of the ALD process. This could lead to a *local* decrease in the

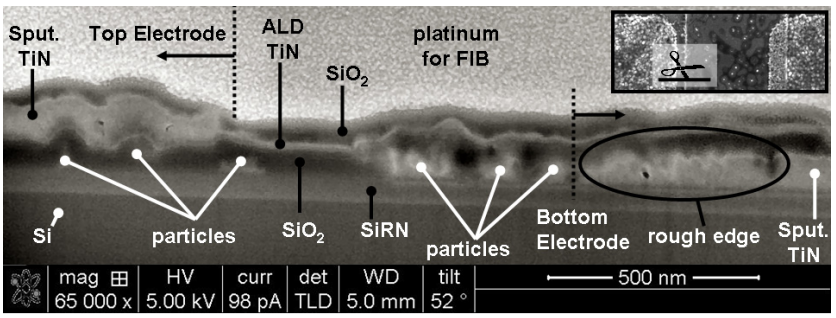


Figure 6.15: HRSEM cross-section, made with the FIB, at the position where the top electrode (horizontal in inset) and bottom electrode (vertical in inset) cross each other. Particles are observed at position where the TiN layer is etched.

oxide thickness and/or lower intrinsic oxide quality. When the average SiO_2 properties are used, the local deviation of the oxide thickness is not accounted for and the actual electric field can be much higher. Hence, high leakage currents and low breakdown fields of the SiO_2 layer in SMAs are extracted (MIM-AP, Figure 6.12). Furthermore, the point-shaped particles near the bottom electrode can lead to a higher electric field [113]. In MIM-1-capacitors, having a PVD top electrode with a worse step coverage, the structural defects are *not contacted* by the top electrode and hence do not deteriorate the electrical characteristics. The MIS-capacitors (MIS-1 and MIS-2) do not have these structural defects, as a result of the non-patterned (flat) silicon bottom electrode. This leads to the good electrical characteristics.

6.6 The origin of the particles

In order to find the origin of the roughness and the particles near the TiN bottom electrode edge, SMAs without a conductive link are investigated at different locations across the wafer (see inset Figure 6.16): near the wafer centre (❸), near the edge (❶) and in between (❷). In Figure 6.16, top-view HRSEM images are shown at these positions. Very little difference is observed visually in the roughness of the bottom electrode edge at location (❶), (❷) and (❸).

Particles are observed in the area where the bottom electrode is etched at location (❷) and (❸) (see close-ups). The particle density decreases from location (❸) to (❷) and, at location (❶), no particles are observed. These are the particles that are covered by SiO_2, as shown in Figure 6.15b.

In Figure 6.17, *IV*-characteristics are shown for these SMAs without link, for a voltage sweep up to 50 mV. Different leakage currents are observed for all the three positions. Starting from location (❶), the leakage current at 50 mV is 10^{-11} A (near the lower measurement limit of the setup) and increases at position (❷) by more than 3 orders of magnitude; from position (❷) to (❸), it increases by another 2 orders of magnitude to the level of 10^{-5} A. This shows that the leakage current is related to the position of the device, and therefore related to the particle density. Namely, the

devices nearer to the wafer centre have a higher particle density and higher leakage current. This result further confirms the correlation between particles and leakage currents, as stated earlier in section 6.5.

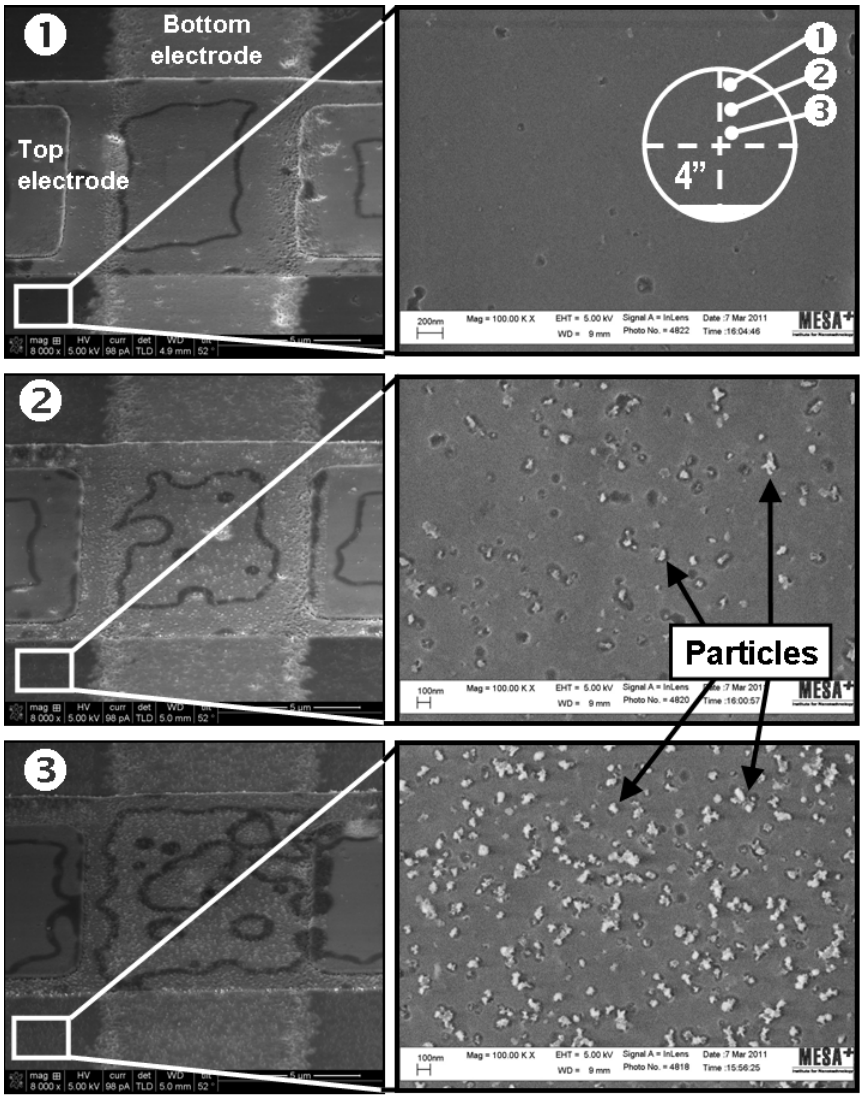


Figure 6.16: HR-SEM images (top-view) of SMAs without a conductive link (bottom electrode horizontal, top electrode vertical) at various device positions on the wafer (see inset top right). Overview (left-hand column) and close-up near the edge of the bottom electrode (right-hand column).

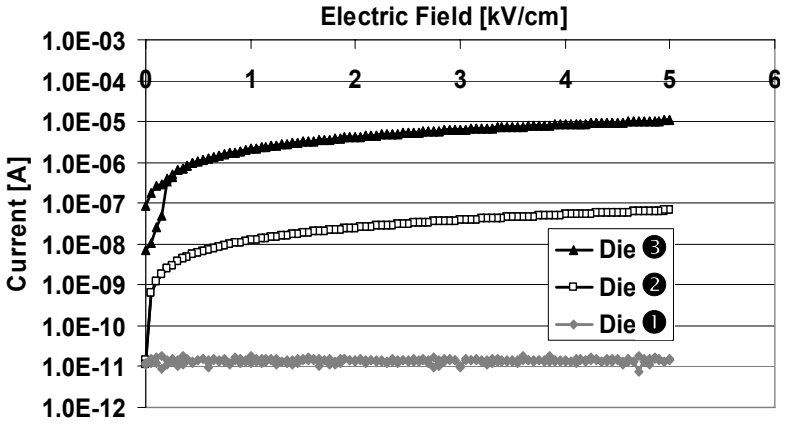


Figure 6.17: IV-characteristics for SMAs without link at various positions across the wafer. Numbers correspond to positions in Figure 6.16a.

The particles are present at positions where the TiN bottom electrode is etched. Therefore, the particles could be the result of improper etching of the TiN layer.

In order to clarify the reason of a lower particle density towards the wafer edge, the layer thickness of bottom electrode is determined as a function of the position on the wafer.

As shown previously in section 2.2.1 (eq. (2.3)), the layer thickness (t) can be extracted from electrical measurements the sheet resistance (R_{sh}) and the resistivity (ρ). R_{sh} is determined from electrical measurements on the Greek Crosses with a design, similar to that shown in Figure 2.8 (section 2.3.2) and they are measured with the same metrology.

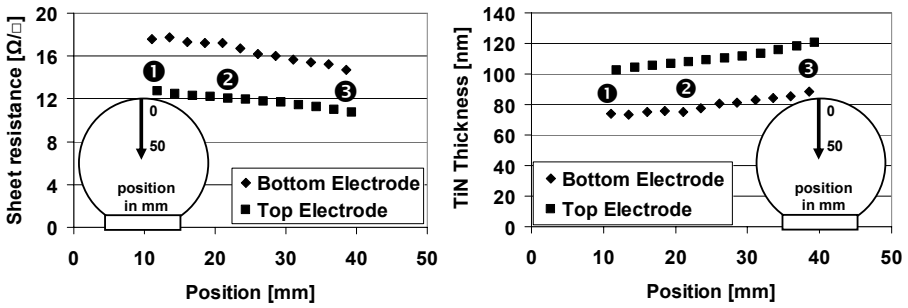
For sputtered bottom electrode TiN layer, the extracted R_{sh}-values are shown as function of the position on the wafer in Figure 6.18a. Lower R_{sh}-values are measured towards the wafer centre. Using equation (2.3) and a resistivity of 130 μΩcm, the layer thickness is calculated and shown as a function of the position on the wafer in Figure 6.18b. The extracted thickness values are in agreement with dektak measurements (not shown). It is observed that the TiN bottom electrode is ca. 15 % thicker at position (❸) (wafer centre) with respect to position (❶) (wafer edge). This is caused by a non-uniform deposition of the TiN layer in the sputtering process, resulting

in variations of the film thickness. In Figure 6.18, data for the sputtered top electrode is shown, which is fabricated using identical fabrication steps as for the bottom electrode. The same trend in R_{sh} and the layer thickness are observed as for the bottom electrode. Although the thickness variation of the top electrode is not relevant for the leakage currents in SMAs, the same thickness variation in the top electrode confirms the non-uniform deposition process as the root-cause for the thickness variation of the bottom electrode.

As both the particle density and the TiN layer thickness are shown to be a function of the position on the wafer, they can be correlated.

TiN is etched using a wet chemical etching process, which means that a thinner TiN layer is etched at position (❶) compared to position (❸) during the same etch time. Assuming that the particles are the parts of the remaining (i.e. not fully etched) TiN layer, they had effectively more time to be removed at position (❶) than position (❸). This could explain the correlation between the particle density and TiN layer thickness of the bottom electrode and hence the relation to high leakage currents in SMAs.

These results indicate that the high leakage currents and low breakdown fields in SMAs are related to the presence of particles at positions where the TiN bottom electrode is not completely etched.



(a) *(b)*

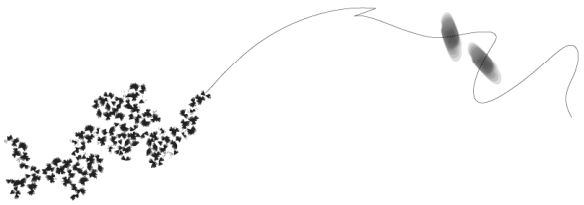
Figure 6.18: Sheet resistance measurements (a) and extracted layer thicknesses (b) for 100 nm thick sputtered TiN top and bottom electrodes. Numbers correspond to positions in Figure 6.16. (0,0) refers to the top edge of the wafer (see inset).

6.7 Conclusions

A sharp decrease in the measured link resistance of 3 orders of magnitude is observed during a voltage sweep for nanolink-based SMAs up at ~2.5 V and for application of a constant voltage of 4.1V for a few seconds. This is the result of dielectric breakdown of the ICPECVD SiO_2 layer in the device. The dielectric breakdown occurs at the edge of the sputtered TiN bottom electrode where the top and bottom electrode cross each other. This leads to the formation of a low Ohmic breakdown part (or anti-fuse) parallel to the nanolink. The dielectric breakdown occurs at an electric field across the SiO_2 layer of 0.25 MV/cm, which is more than 1 order of magnitude lower than for high quality SiO_2 layers. SMAs without a conductive link have the same low breakdown field and high (sub-breakdown) leakage currents. The leakage currents are not related to the width or area of the SMAs.

Using electrical measurements on MIS- and MIM-capacitors, it is shown that the high leakage currents and the low breakdown fields of the ICPECVD SiO_2 layer are not related to the intrinsic SiO_2 quality, but are an intrinsic feature of devices with a patterned sputtered TiN bottom electrode in combination with the presence of ALD TiN layer for the top electrode. A combination of HRSEM and FIB analysis showed the presence of particles at positions where the sputtered bottom TiN electrode is etched. A correlation between the particle density and high leakage currents is shown. It is proposed that high leakage currents and low breakdown fields are the result of structural defects in the SiO_2 layer, caused by remaining TiN particles. The defects are filled by the ALD TiN layer, leading different oxide properties and a thinner oxide layer locally. The particles are most likely the result of improper etching of the bottom TiN layer and are related to the etching time of the TiN layer. The structural defects in the SiO_2 layer are electrically contacted only in case of an ALD TiN top electrode and hence lead to high leakage currents and low breakdown fields in SMAs.

7 Conclusions and recommendations



7.1 Conclusions

In this work, we investigated a new fabrication process for ultralow power, microelectronic thermal devices, based on the deposition of an ultrathin (7-15 nm) titanium nitride (TiN) layer via atomic layer deposition (ALD). The device consists of a nanolink which is electrically heated by Joule heating. It is called the nanolink-based suspended membrane actuator (SMA). The nanolink is a cylindrically shaped conductive volume, that is embedded in an SiO_2 layer, sandwiched between two sputtered TiN electrodes. The nanolink is fabricated by first etching a nanoscopic hole (∅ 100 nm) in an SiO_2 layer covering the TiN bottom electrode and subsequent filling with the ALD TiN thin film ('drill-and-fill' process). In this way, the TiN electrodes are electrically connected via the nanolink.

SMAs can be used for a variety of applications, based on both generating a hot area at the surface and measuring the temperature change due to interaction with the ambient. This means the nanolink simultaneously acts as a thermal actuator and thermal sensor. Therefore, the electrical resistance or resistivity (ρ) and the temperature coefficient of resistance (TCR) of the ALD TiN thin film are of prime importance.

Special four-point microelectronic test structures were designed and realized to measure the resistance and TCR of ultra-thin ALD TiN layers on a flat surface. The resistivity and TCR of 4-15 nm thick ALD TiN films were obtained successfully in the temperature (T) range of 25-175 ºC using these test structures. The extracted ρ-and TCR-values are found to be related to the layer thickness. Thinner ALD TiN layers have a higher resistivity and lower TCR values. Furthermore, the TCR is measured at temperatures up to 700 ºC using test structures on silicon and quartz substrates. A linear $R(T)$-relation is obtained for temperatures up to 600 ºC. The TCR of ALD TiN thin films, extracted between 25-175 ºC, can be used successfully to determine device temperatures up to 600 ºC

During fabrication and operation of the SMA at elevated temperatures and in oxidizing ambient, the ALD TiN layer should not oxidize. The plasma-assisted (25-300 ºC) and thermal oxidations (300-500 ºC) of ALD TiN layers at atmospheric conditions in dry (O_2) and wet (H_2O) ambient are investigated. For thermal oxidation, two regimes, initial (fast) and 2nd (parabolic), are distinguished. The extracted activation energies for the parabolic regime are in agreement with the literature values known for stoichiometric sputtered TiN layers. For plasma oxidation in an N_2O plasma, also two time regimes are distinguished: fast (and temperature independent) and slow (with increased oxidation rate at higher temperatures). This is an indication of two different oxidation mechanisms.

The materials analysis shows that as-deposited ALD TiN is stoichiometric within 10 % and it contains small fractions of Cl and H. EFTEM of partly oxidized TiN exhibits gradual N- and O-concentration profiles across the layer thickness, pointing to the enhanced grain-boundary diffusion. Fully oxidized TiN consists of stoichiometric TiO_2.

Oxidation of TiN films can be avoided by the deposition of a blocking or passivation layer, to stop oxidizing species getting in contact with the TiN surface. Samples passivated with 25-50 nm (IC)PECVD SiO_2 or Si_3N_4 and ALD Al_2O_3 layers showed no significant oxidation in wet ambient at temperatures up to 500 ºC for 28 hours. During the plasma enhanced CVD of SiO_2, however, the underlying TiN oxidizes significantly (i.e. a few nm of TiO_2 are formed) during the first minute of deposition. This makes SiO_2 less suitable as a passivation layer for ultrathin ALD TiN films.

SMAs with micro- (∅ 2-6 μm) and nanolinks (∅ 100 nm) have been realized successfully. The electrical characteristics of the devices in terms of the link resistance (R_{link}) are discussed using an electrical model, consisting of the resistance of the (cylindrically-shaped) ALD TiN film (R_{cyl}) in series with the (metal-to-metal) contact resistance of the ALD TiN film with the bottom electrode (R_{cont}). The actual link temperature is estimated using (the change in) the link resistance and the TCR of the link.

Microlink-based SMAs have a link resistance of ~40 Ω. It is dominated by R_{cyl} and shows a positive TCR of the flat ALD TiN layer. A link temperature of ~250 ºC can be reached at a power consumption of 2.7 mW in the link.

Nanolink-based SMAs have nanosized (∅ 100 nm) links with a link resistance of ~7 MΩ. It is dominated by R_{cont} and shows a negative TCR. A link temperature of ~280 ºC is obtained with a power consumption of 5.5 µW. This is more than 2 orders of magnitude lower than microlink-based SMAs, and antifuse-based SMAs that are previously reported by Kovalgin et.al [2].

Two techniques, infrared (IR) thermometry and polymer melting were investigated to determine the temperature of SMAs, independent from the electrical method.

IR thermometry can be used successfully to determine the temperature of microlink-based SMAs. The extracted temperature is in excellent agreement with the electrically measurement link temperature. The polymer melting technique can be applied successfully to large area meander shaped heaters. However, both IR thermometry and polymer melting techniques, as employed in this thesis, are not sensitive enough to measure the temperature of the nanolink.

For some devices, the high quality ICPECVD silicon oxide (SiO_2) layer between the sputtered electrodes, loses its insulating properties (dielectric breakdown) and exhibits high leakage currents at unexpectedly low electric fields ($E_{BD,SiO2} < 0.5$ MV/cm). The application of an ALD TiN layer on top of a dielectric layer is demonstrated to induce electrical failures. It is the root-cause for the observed electrical behaviour. Based on HRSEM and FIB analysis, it was shown that the low electric breakdown field and the high leakage currents are the result of structural defects in the SiO_2 layer, electrically enhanced by the ALD layer.

7.2 Recommendations

The design of the nanolink-based SMA, as described in section 4.2.1, is based on earlier work by Kovalgin *et al.* [2]. It is used as a starting point to test the feasibility of the proposed fabrication method for the nanolink with ALD TiN (i.e. the 'drill-and-fill' process).The performance of SMAs in terms of power dissipation and maximum temperature can be improved by minimizing the heat losses of the nanolink to the substrate and to the connection leads. The use of quartz substrates provides maintaining of CMOS compatibility in combination with a lower heat conductivity and heat capacity compared to silicon. An increase of the thermal resistance of the connection leads can significantly minimize heat losses. In this respect the design and technology can be optimized by increasing the actual link resistance, which allows scaling of the connection leads, while satisfying a high link to connection resistance ratio.

In the case of crossing electrodes configurations, the use of ALD TiN on dielectric layers is prone to electrical leakage failures. This is caused by structural defects in the dielectric layer in combination with the ALD TiN deposition. To circumvent the electric failures in the SiO_2 layer and crossing electrodes, a nanolink design is recommended where the link is situated in one plane (i.e. one layer) with the connection electrodes. This lateral approach is basically a miniaturization of the classic meander shaped heater. Technological capabilities like advanced lithography and patterning techniques and passivated ALD-type films, as shown in the present work, are the prerequisites.

In chapter 5 it is concluded that the IR thermometry technique is not sensitive enough to measure the temperature of the nanolink in the present setup. It can be improved by using mid wave IR (λ = 3 – 5 μm) [129] that captures the peak in the spectrum (Planck curve) with a higher IR intensity in the temperature range of 300 – 700 °C. Merging a probe station, a thermochuck and this IR setup facilitates characterization of a variety of devices at elevated temperatures without the need for separate calibration devices.

References

[1] A. Y. Kovalgin, J. Holleman, and G. Iordache, "A Pillar-Shaped Antifuse-Based Silicon Chemical Sensor and Actuator," IEEE Sensors Journal, vol. 7, pp. 18-27, 2007.

[2] A. Y. Kovalgin, J. Holleman, G. Iordache, T. Jenneboer, F. Falke, V. Zieren, and M. J. Goossens, "Low-power, antifuse-based silicon chemical sensor on a suspended membrane," Journal of the Electrochemical Society, vol. 153, pp. H181-H188, 2006.

[3] M. Gall, "Si planar pellistor. A low-power pellistor sensor in Si thin-film technology," Sensors and Actuators, B: Chemical, vol. B4, pp. 533-538, 1991.

[4] C. Ducso, M. Adam, P. Furjes, M. Hirschfelder, S. Kulinyi, and I. Barsony, "Explosion-proof monitoring of hydrocarbons by mechanically stabilised, integrable calorimetric microsensors," Sensors and Actuators, B: Chemical, vol. 95, pp. 189-194, 2003.

[5] I. Simon, N. Barsan, M. Bauer, and U. Weimar, "Micromachined metal oxide gas sensors: opportunities to improve sensor performance," Sensors and Actuators B: Chemical, vol. 73, pp. 1-26, 2001.

[6] P. Furjes, C. Ducso, M. Adam, J. Zettner, and I. Barsony, "Thermal characterisation of micro-hotplates used in sensor structures," Superlattices and Microstructures, vol. 35, pp. 455-464, 2004.

[7] H. E. de Bree, "An overview of microflown technologies," Acta Acustica United with Acustica, vol. 89, pp. 163-172, 2003.

[8] R. M. Tiggelaar and J. G. E. Gardeniers, "Silicon and Glass Microreactors," in *Micro Process Engineering*, vol. 2, V. Hessel, A. Renken, J. C. Schouten, and J. Yoshida, Eds. Weinheim: Wiley-VCH, 2009, 978-3-527-31550-5.

[9] T. A. Jones and P. T. Walsh, "Flammable Gas Detection: the role of the platinum metals," Platinum Metals Review, vol. 32, pp. 50-60, 1988.

[10] M. Abbaspour and N. Mansouri, "City hazardous gas monitoring network," Journal of Loss Prevention in the Process Industries, vol. 18, pp. 481-487, 2005.

[11] P. T. Moseley and B. C. Tofield, *Solid State Gas Sensors*. Bristol: IOP Publishing Ltd, Technohouse, Redcliffe Way, Bristol BS1 6NX, England, 1987, 0-85274-514-1.

[12] W. Tsujita, A. Yoshino, H. Ishida, and T. Moriizumi, "Gas sensor network for air-pollution monitoring," Sensors and Actuators B: Chemical, vol. 110, pp. 304-311, 2005.

[13] J. Watson, "The tin oxide gas sensor and its applications," Sensors and Actuators, vol. 5, pp. 29-42, 1984.

[14] B. H. Weiller, P. D. Fuqua, and J. V. Osborn, "Fabrication, Characterization, and Thermal Failure Analysis of a Micro Hot Plate Chemical Sensor Substrate," Journal of the Electrochemical Society, vol. 151, 2004.

[15] S. Kulinyi, D. Brandszajsz, H. Amine, M. Adam, P. Furjes, I. Barsony, and C. Ducso, "Olfactory detection of methane, propane, butane and hexane using conventional transmitter norms," Sensors and Actuators B: Chemical, vol. 111, pp. 286-292, 2005.

[16] M. Gall, "The Si-Planar-Pellistor array, a detection unit for combustible gases," Sensors and Actuators B: Chemical, vol. 16, pp. 260-264, 1993.

[17] P. Kurzawski, C. Hagleitner, and A. Hierlemann, "Detection and discrimination capabilities of a multitransducer single-chip gas sensor system," Analytical Chemistry, vol. 78, pp. 6910-6920, 2006.

[18] S. Ampuero and J. O. Bosset, "The electronic nose applied to dairy products: a review," Sensors and Actuators B: Chemical, vol. 94, pp. 1-12, 2003.

[19] S. M. Lee, D. C. Dyer, and J. W. Gardner, "Design and optimisation of a high-temperature silicon micro-hotplate for nanoporous palladium pellistors," Microelectronics Journal, vol. 34, pp. 115-126, 2003.

[20] J. A. Stankovic, "Wireless Sensor Networks," Computer, vol. 41, pp. 92-95, 2008.

[21] P. N. Bartlett and S. Guerin, "A micromachined calorimetric gas sensor: an application of electrodeposited nanostructured palladium for the detection of combustible gases," Analytical Chemistry, vol. 75, pp. 126-132, 2003.

[22] R. M. Tiggelaar, P. v. Male, J. W. Berenschot, J. G. E. Gardeniers, R. E. Oosterbroek, M. H. J. M. d. Croon, J. C. Schouten, A. v. d. Berg, and M. C. Elwenspoek, "Fabrication of a high-temperature microreactor with integrated heater and sensor patterns on an ultrathin silicon membrane," Sensors and Actuators A: Physical, vol. 119, pp. 196-205, 2005.

[23] J. R. McBride, K. E. Nietering, and K. R. Ellwood, "Design considerations for optimizing the sensitivity of catalytic calorimetric gas sensors: modeling and experimental results," Sensors and Actuators B-Chemical, vol. 73, pp. 163-173, 2001.

[24] G. Veser, M. Ziauddin, and L. D. Schmidt, "Ignition in alkane oxidation on noble-metal catalysts," Catalysis Today, vol. 47, pp. 219-228, 1999.

[25] M. Caron, M. Goethals, G. De Smedt, J. Berghmans, S. Vliegen, E. Van't Oost, and A. van den Aarssen, "Pressure dependence of the auto-ignition temperature of methane/air mixtures," Journal of Hazardous Materials, vol. 65, pp. 233-244, 1999.

[26] S. Z. Ali, F. Udrea, W. I. Milne, and J. W. Gardner, "Tungsten-Based SOI Microhotplates for Smart Gas Sensors," Journal of Microelectromechanical Systems, vol. 17, pp. 1408-1417, 2008.

[27] The E2V website: www.e2v.com

[28] D. K. Y. Liu, K. Chen, H. Tigelaar, J. Paterson, and S. O. Chen, "Scaled dielectric antifuse structure for field-programmable gate array applications," Electron Device Letters, IEEE, vol. 12, pp. 151-153, 1991.

[29] J. Kim and K. Lee, "3-Transistor antifuse OTP ROM array using standard CMOS process," in Proc. Symposium on VLSl Circuits, 2003, pp. 239-242.

[30] H. K. Cha, I. Yun, J. Kim, B. C. So, K. Chun, I. Nam, and K. Lee, "A 32-KB standard CMOS antifuse one-time programmable ROM embedded in a 16-bit microcontroller," IEEE Journal of Solid-State Circuits, vol. 41, pp. 2115-2124, 2006.

[31] T. Hoang, "High Efficiency Infrared-Light Emission From Silicon LEDs", PhD thesis, 2007, University of Twente.

[32] G. Piccolo, H. Tu, J. Holleman, A. Y. Kovalgin, and J. Schmitz, "Silicon LEDs with antifuse injection," in Proc. 5th IEEE International Conference on Group IV Photonics, 2008, pp. 49-51.

[33] F. Hawley, F. Issaq, J. Ranaweera, R. Lambertson, and J. McCollum, "Metal containing link formed in amorphous silicon metal-to-metal antifuse," in Proc. Materials Research Society Symposium, 2003, pp. 699-704.

[34] T. Yeoh, N. Ives, N. Presser, G. Stupian, M. Leung, J. McCollum, and F. Hawley, "Analysis of Successive Focused Ion Beam Slices by Scanning Electron Imaging and 3D Reconstruction," in Proc. Materials Research Society 2005 Fall meeting, 2005, pp. 11.1-11.6.

[35] S. T. Smith and R. M. Seugling, "Sensor and actuator considerations for precision, small machines," Precision Engineering, vol. 30, pp. 245-264, 2006.

[36] J. M. Camacho and A. I. Oliva, "Surface and grain boundary contributions in the electrical resistivity of metallic nanofilms," Thin Solid Films, vol. 515, pp. 1881-1885, 2006.

[37] E. Pop, S. Sinha, and K. E. Goodson, "Heat generation and transport in nanometer-scale transistors," Proceedings of the IEEE, vol. 94, pp. 1587-1601, 2006.

[38] F. J. Jedema, NXP Eindhoven, *private communication*, 2009.

[39] S. A. Campbell, *The Science and Engineering of Microfabrication*, 2nd ed. New York: Oxford University Press, 2001, 0-19-513605-5.

[40] M. Graf, U. Frey, S. Taschini, and A. Hierlemann, "Micro hot plate-based sensor array system for the detection of environmentally relevant gases," Analytical Chemistry, vol. 78, pp. 6801-6808, 2006.

[41] I. Brunets, "Electronic Devices fabricated at CMOS backend-compatible Temperatures", PhD thesis, 2009, University of Twente.

[42] J. Schmitz, "Adding functionality to microchips by wafer post-processing," Nuclear instruments and methods in physics research. Section A, Accelerators, spectrometers, detectors and associated equipment, vol. 576, pp. 142-149, 2007.

[43] J. F. Creemer, W. van der Vlist, C. R. de Boer, H. W. Zandbergen, P. M. Sarro, D. Briand, and N. F. de Rooij, "MEMS hotplates with TiN as a heater material," IEEE Sensors, pp. 4, 2005.

[44] S. B. S. Heil, E. Langereis, F. Roozeboom, M. C. M. van de Sanden, and W. M. M. Kessels, "Low-temperature deposition of TiN by plasma-assisted atomic layer deposition," Journal of the Electrochemical Society, vol. 153, pp. G956-G965, 2006.

[45] N. Yokoyama, K. Hinode, and Y. Homma, "LPCVD titanium nitride for ULSIs," Journal of the Electrochemical Society, vol. 138, pp. 190-195, 1991.

[46] H. G. Tompkins, J. A. Sellers, and C. Tracy, "An Inorganic Antireflective Coating for Use in Photolithography," Journal of Applied Physics, vol. 73, pp. 3932-3938, 1993.

[47] M. C. Lemme, J. K. Efavi, T. Mollenhauer, M. Schmidt, H. D. B. Gottlob, T. Wahlbrink, and H. Kurz, "Nanoscale TiN metal gate technology for CMOS integration," Microelectronic Engineering, vol. 83, pp. 1551-1554, 2006.

[48] Y. Yin, L. Hang, S. Zhang, and X. L. Bui, "Thermal oxidation properties of titanium nitride and titanium-aluminum nitride materials - A perspective for high temperature air-stable solar selective absorber applications," Thin Solid Films, vol. 515, pp. 2829-2832, 2007.

[49] P. de Moor, A. Witvrouw, V. Simons, and I. de Wolf, "The Fabrication of Reliability Testing of Ti/TiN heaters," in Proc. SPIE, 1999, pp. 284-293.

[50] W. M. Heuvelman, P. Helderman, G. C. A. M. Janssen, and S. Radelaar, "TiN reactive sputter deposition studied as a function of the pumping speed," Thin Solid Films, vol. 332, pp. 335-339, 1998.

[51] M. J. Buiting, A. F. Otterloo, and A. H. Montree, "Kinetic Aspects of the Lpcvd of Titanium Nitride from Titanium Tetrachloride and Ammonia," Journal of the Electrochemical Society, vol. 138, pp. 500-505, 1991.

[52] N. Kumar, K. Pourrezaei, M. Fissel, T. Begley, B. Lee, and E. C. Douglas, "Growth and properties of radio frequency reactively sputtered titanium nitride thin films," Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, vol. 5, pp. 1778, 1987.

[53] E. Langereis, S. B. S. Heil, M. C. M. van de Sanden, and W. M. M. Kessels, "In situ spectroscopic ellipsometry study on the growth of ultrathin TiN films by plasma-assisted atomic layer deposition," Journal of Applied Physics, vol. 100, pp. 023534, 2006.

[54] H. Z. Durusoy, O. Duyar, A. Aydinli, and F. Ay, "Influence of substrate temperature and bias voltage on the optical transmittance of TiN films," Vacuum, vol. 70, pp. 21-28, 2003.

[55] S. R. Wilson, C. J. Tracy, and J. L. Freeman Jr, *Handbook of multilevel metallization for integrated circuits: material, technology and applications*. New Jersey: Noyes publications, 1993, 0-8155-1340-2.

[56] J. L. Vossen and W. Kern, *Thin Film Processes II*, 2nd ed. Boston: Academic Press, 1991, 0-12-728251-3.

[57] M. Ritala and M. Leskelä, "Ch. 2: Atomic layer deposition," in *Handbook of thin film materials part 1: Deposition and processing of thin films*, vol. 1, H. S. Nalwa, Ed.: Academic Press, 2002, pp. 103-159, 0-12-512909-2.

[58] J. H. Klootwijk, K. B. Jinesh, W. Dekkers, J. F. Verhoeven, F. C. van den Heuvel, H. D. Kim, D. Blin, M. A. Verheijen, R. Weemaes, M. Kaiser, J. Ruigrok, and F. Roozeboom, "Ultrahigh Capacitance Density for Multiple ALD-Grown MIM Capacitor Stacks in 3-D Silicon," IEEE Electron Device Letters, vol. 29, pp. 740-742, 2008.

[59] J. W. Elam, D. Routkevitch, P. P. Mardilovich, and S. M. George, "Conformal Coating on Ultrahigh-Aspect-Ratio Nanopores of Anodic Alumina by Atomic Layer Deposition," Chemistry of Materials, vol. 15, pp. 3507-3517, 2003.

[60] M. J. Madou, *Fundamentals of microfabrication : the science of miniaturization*, 2nd edition ed: Boca Raton : CRC Press, 2002, 0-8493-0826-7.

[61] R. G. Bankras, "In-situ RHEED and characterization of ALD Al2O3 gate dielectrics (PhD thesis)", PhD thesis, 2006, University of Twente.

[62] H. van Bui, A. W. Groenland, A. A. I. Aarnink, R. A. M. Wolters, and J. Schmitz, "Growth Kinetics and Oxidation Mechanism of ALD TiN Thin Films Monitored by In Situ Spectroscopic Ellipsometry," Journal of the Electrochemical Society, vol. 158, pp. 214-220, 2011.

[63] A. Boogaard, A. Y. Kovalgin, I. Brunets, A. A. I. Aarnink, J. Holleman, R. A. M. Wolters, and J. Schmitz, "Characterization of SiO2 films deposited at low temperature by means of remote ICPECVD," Surface and Coatings Technology, vol. 201, pp. 8976-8980, 2007.

[64] A. Boogaard, A. Kovalgin, T. Aarnink, R. Wolters, J. Holleman, I. Brunets, and J. Schmitz, "Langmuir-probe Characterization of an Inductively-Coupled Remote Plasma System intended for CVD and ALD," ECS Transactions, vol. 2, pp. 181-191, 2007.

[65] A. Boogaard, A. Y. Kovalgin, and R. A. M. Wolters, "Net negative charge in low-temperature SiO2 gate dielectric layers," Microelectronic Engineering, vol. 86, pp. 1707-1710, 2009.

[66] H. Van Bui, A. W. Groenland, A. A. I. Aarnink, R. A. M. Wolters, J. Schmitz, and A. Y. Kovalgin, "Growth Kinetics and Oxidation Mechanism of ALD TiN Thin Films Monitored by In Situ Spectroscopic Ellipsometry," Journal of The Electrochemical Society, vol. 158, pp. H214-H220, 2010.

[67] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed: Wiley-Interscience, 2006, 978-0-471-73906-7.

[68] L. van der Pauw, "A Method of Measuring Specific Resistivity and Hall Effect of Discs of Arbitrary Shape," Philips Research Reports, vol. 13, pp. 1-9, 1958.

[69] M. G. Buehler and W. R. Thurber, "An Experimental Study of Various Cross Sheet Resistor Test Structures," Journal of The Electrochemical Society, vol. 125, pp. 645-650, 1978.

[70] W. Versnel, "Analysis of symmetrical Van der Pauw structures with finite contacts," Solid-State Electronics, vol. 21, pp. 1261-1268, 1978.

[71] N. M. P. Guillaume, M. W. Cresswell, R. A. Allen, S. Everist, and L. W. Linholm, "Comparison of sheet-resistance measurements obtained by standard and small-area four-point probing," in Proc. IEEE ICMTS, 1999, pp. 62-66.

[72] L. van der Pauw, "A method of measuring the resistivity and Hall coefficient on lamellae of arbitrary shape," Philips Technical Review, vol. 20, pp. 220-224, 1958.

[73] Y. Sun, J. Shi, and Q. Meng, "Measurement of sheet resistance of cross microareas using a modified van der Pauw method," Semiconductor Science and Technology, vol. 11, pp. 805-811, 1996.

[74] G. P. Carver, R. L. Mattis, and M. G. Buehler, "Design Consideration for the Cross-Bridge Sheet Resistor, NBSIR 82-2548." Washington DC: National Bureau of Standards, 1982.

[75] S. Smith, "Sheet Resistance and Electrical Linewidth Test Structures for Semiconductor Process Characterisation", PhD thesis, 2003, University of Edinburgh, Scotland.

[76] A. Bid, A. Bora, and A. K. Raychaudhuri, "Temperature dependence of the resistance of metallic nanowires of diameter >= 15 nm: Applicability of Bloch-Gruneisen theorem," Physical Review B, vol. 74, 2006.

[77] R. C. Weast, *CRC Handbook of Chemistry and Physics*, 1st student ed: CRC Press, Inc., Boca Raton, Florida, USA, 1987, 0-8493-0740-06.

[78] S. Enderling, C. L. Brown, III, S. Smith, M. H. Dicks, J. T. M. Stevenson, M. Mitkova, M. N. Kozicki, and A. J. Walton, "Sheet resistance measurement of non-standard cleanroom materials using suspended Greek cross test structures," IEEE Transactions on Semiconductor Manufacturing, vol. 19, pp. 2-9, 2006.

[79] L. Giraudet, S. Fauveaux, O. Simonetti, C. Petit, K. Blary, T. Maurel, and A. Belkhir, "Spin-coated conductive polymer film resistivity measurement using the TLM method," Synthetic Metals, vol. 156, pp. 838-842, 2006.

[80] S. Bystrova, A. A. I. Aarnink, J. Holleman, and R. A. M. Wolters, "Atomic Layer Deposition of W[sub 1.5]N Barrier Films for Cu Metallization," Journal of The Electrochemical Society, vol. 152, pp. G522-G527, 2005.

[81] D. S. Perloff, "Four-point sheet resistance correction factors for thin rectangular samples," Solid-State Electronics, vol. 20, pp. 681-687, 1977.

[82] S. Smith and A. J. Walton, SMC Edinburgh, *private communication*, 2010.

[83] J. E. Sundgren, "Structure and properties of TiN coatings," Thin Solid Films, vol. 128, pp. 21-44, 1985.

[84] K. Fuchs, "The conductivity of thin metallic films according to the electron theory of metals," Mathematical Proceedings of the Cambridge Philosophical Society, vol. 34, pp. 100-108, 1938.

[85] S. B. Soffer, "Statistical Model for the Size Effect in Electrical Conduction," Journal of Applied Physics, vol. 38, pp. 1710-1715, 1967.

[86] P. Patsalas and S. Logothetidis, "Optical, electronic, and transport properties of nanocrystalline titanium nitride thin films," Journal of Applied Physics, vol. 90, pp. 4725-4734, 2001.

[87] T. J. Mouthaan, *Semiconductor Devices Explained using active simulation*. Chichester: John Wiley & Sons Ltd, 1999, 0-471-98854-5.

[88] S. M. Sze and K. K. NG, *Physics of semiconductor devices*, 3rd ed. New Jersey: Wiley, 2007, 978-0-471-14323-9.

[89] D. B. M. Klaassen, "A unified mobility model for device simulation--II. Temperature dependence of carrier mobility and lifetime," Solid-State Electronics, vol. 35, pp. 961-967, 1992.

[90] C. Corvasce, M. Ciappa, D. Barlini, F. Illien, and W. Fichtner, "Measurement of the silicon resistivity at very high temperature with junction isolated van der Pauw structures," in Proc. IEEE ICMTS, 2004, pp. 133-138 Vol.1.

[91] P. S. Maiya and B. M. Moon, "Properties of TiN and TiN deposited by CVD on graphite for pyrochemical applications," in Proc. Material Research Society Symposium, 1998, pp. 01998.

[92] H. Itoh, K. Kato, and K. Sugiyama, "Chemical vapour deposition of corrosion-resistant TiN film to the inner walls of long steel tubes," Journal of Materials Science, vol. 21, pp. 751-756, 1986.

[93] B. Y. Kim, S. H. Lee, S. G. Park, K. Y. Oh, J. Song, and D. H. Kim, "Comparison Study for TiN Films Deposited from Different Method: Chemical Vapor Deposition and Atomic Layer Deposition," in Proc. Material Research Society Symposium, 2001, pp.

[94] I. Suni, D. Sigurd, K. T. Ho, and M. A. Nicolet, "Thermal oxidation of reactively sputtered titanium nitride and hafnium nitride films," Journal of the Electrochemical Society, vol. 130, pp. 1210-1214, 1983.

[95] M. Wittmer, J. Noser, and H. Melchior, "Oxidation-Kinetics of Tin Thin-Films," Journal of Applied Physics, vol. 52, pp. 6659-6664, 1981.

[96] S. Logothetidis, E. I. Meletis, G. Stergioudis, and A. A. Adjaottor, "Room temperature oxidation behavior of TiN thin films," Thin Solid Films, vol. 338, pp. 304-313, 1999.

[97] E. Langereis, S. B. S. Heil, H. C. M. Knoops, W. Keuning, M. C. M. van de Sanden, and W. M. M. Kessels, "In situ spectroscopic ellipsometry as a versatile tool for studying atomic layer deposition," Journal of Physics D: Applied Physics, vol. 42, pp. 073001, 2009.

[98] B. E. Deal and A. S. Grove, "General Relationship for the Thermal Oxidation of Silicon," Journal of Applied Physics, vol. 36, pp. 3770-3778, 1965.

[99] A. Y. Kovalgin, A. J. Hof, and J. Schmitz, "An approach to modeling of silicon oxidationin a wet ultra-diluted ambient," Microelectronic Engineering, vol. 80, pp. 432-435, 2005.

[100] A. Y. Kovalgin, A. Zinine, R. Bankras, H. Wormeester, B. Poelsema, and J. Schmitz, "On the Growth of Native Oxides on Hydrogen-Terminated Silicon Surfaces in Dark and Under Illumination with Light," ECS Transactions, vol. 3, pp. 191-202, 2006.

[101] G. G. Fountain, S. V. Hattangady, R. A. Rudder, R. J. Markunas, G. Lucovsky, S. S. Kim, and D. V. Tsu, "Evidence for the occurrence of subcutaneous oxidation during low temperature remote plasma enhanced deposition of silicon dioxide films," Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, vol. 7, pp. 576-580, 1989.

[102] A. Masuda, A. Morimoto, M. Kumeda, T. Shimizu, Y. Yonezawa, and T. Minamikawa, "Novel oxidation process of hydrogenated amorphous silicon utilizing nitrous oxide plasma," Applied Physics Letters, vol. 61, pp. 816-818, 1992.

[103] R. A. M. Wolters, *private communication*, 2011.

[104] J. Desmaison, P. Lefort, and M. Billy, "Oxidation mechanism of titanium nitride in oxygen," Oxidation of Metals, vol. 13, pp. 505-517, 1979.

[105] M. Maeda, T. Yamada, and T. Watanabe, "Photocatalytic Properties of Plasma-Nitrided TiO[sub 2] Films," Journal of The Electrochemical Society, vol. 154, pp. P29-P31, 2007.

[106] R. Kraft, T. P. Schneider, W. W. Dostalik, and S. Hattangady, "Surface nitridation of silicon dioxide with a high density nitrogen plasma," Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, vol. 15, pp. 967-970, 1997.

[107] A. W. Groenland, R. A. M. Wolters, A. Y. Kovalgin, and J. Schmitz, "Four point probe structures with buried electrodes for the electrical characterization of ultrathin conducting films," in Proc. IEEE ICMTS, 2009, pp. 191-195.

[108] N. Stavitski, J. H. Klootwijk, H. W. van Zeijl, A. Y. Kovalgin, and R. Wolters, "Cross-Bridge Kelvin Resistor Structures for Reliable Measurement of Low Contact Resistances and Contact Interface Characterization," IEEE Transactions on Semiconductor Manufacturing, vol. 22, pp. 146-152, 2009.

[109] T. Schwamb, B. R. Burg, N. C. Schirmer, and D. Poulikakos, "On the effect of the electrical contact resistance in nanodevices," Applied Physics Letters, vol. 92, pp. 243106-3, 2008.

[110] M. Elwenspoek and H. Jansen, *Silicon micromachining*. Cambridge: Cambridge University Press, 1998, 0-521-59054-X.

[111] R. Müller-Fiedler and V. Knoblauch, "Reliability aspects of microsensors and micromechatronic actuators for automotive applications," Microelectronics Reliability, vol. 43, pp. 1085-1097, 2003.

[112] B. Bushan, "Part G: 52. Failure Mechanisms in MEMS/NEMS Devices," in *Springer Handbook of Nanotechnology*, B. Bushan, Ed., 2nd ed. Berlin: Springer, 2007, pp. 1663-1664, 3-540-29855-x.

[113] R. P. Feynman, R. B. Leighton, and M. L. Sands, *The Feynman lectures on physics / Feynman, Leighton, Sands*. Redwood City, California: Addison-Wesley, 1989, 0-201-02117-x.

[114] P. R. N. Childs, *Practical Temperature Measurement*. Oxford: Butterworth-Heinemann, 2001, 0-7506-5080-x.

[115] P. R. N. Childs, J. R. Greenwood, and C. A. Long, "Review of temperature measurement," Review of Scientific Instruments, vol. 71, pp. 2959-2978, 2000.

[116] A. v. d. Bos, Sensata Technologies, *private communication*, 2010.

[117] M. Quinn Brewster, *Thermal Radiative Transfer & Properties*: Wiley-Interscience, 1992, 0-471-53982-1.

[118] H. Fischer, "Thermal probe surface treatment of a bulk polymer: Does a surface layer with a lower glass transition than the bulk exist?," Macromolecules, vol. 35, pp. 3592-3595, 2002.

[119] H. Fischer, "Calibration of micro-thermal analysis for the detection of glass transition temperatures and melting points - Repeatability and reproducibility," Journal of Thermal Analysis and Calorimetry, vol. 92, pp. 625-630, 2008.

[120] Y. Nakagawa, R. Schafer, and H. J. Guntherodt, "Picojoule and submillisecond calorimetry with micromechanical probes," Applied Physics Letters, vol. 73, pp. 2296-2298, 1998.

[121] Y. L. Rastorguev, G. F. Bogatov, and B. A. Grigor'ev, "Thermal conductivity of higher n-alkanes," Chemistry and Technology of Fuels and Oils, vol. 10, pp. 728-732, 1974.

[122] J. M. Gordon and M. Huleihil, "General performance characteristics of real heat engines," Journal of Applied Physics, vol. 72, pp. 829-837, 1992.

[123] The Sigma Alltrich product catalog (online), product nr 91447 website: http://www.sigmaaldrich.com/

[124] P. Kulha, A. Boura, and M. Husak, "Design and Fabrication of Piezoresistive Strain-Gauges for Harsh Environment Applications," in Proc. International Conference on Renewable Energies and Power Quality, 2010, pp. 510-513.

[125] C. M. L. Atkinson, J. A. Larkin, and M. J. Richardson, "Enthalpy changes in molten n-alkanes and polyethylene," The Journal of Chemical Thermodynamics, vol. 1, pp. 435-440, 1969.

[126] The US Chemical Handbook website: http://us.chemicalbook.com/

[127] The NIST material library website: http://webbook.nist.gov/

[128] P. Barbillon, L. Schuffenecker, J. Dellacherie, D. Balesdent, and M. Dirande, "Variation d'enthalpie subie de 260 K a 340 K par les n-paraffines, comprises entrel'octadecane et l'hexacosane," J. Chim. Phys. Phys.-Chim. Biol., pp. 91-113, 1991.

[129] J. McDonald, "Optical Microscopy," in *Microelectronics failure analysis, desk reference*, E. D. R. Committee, Ed., 5th ed: ASM International, 2004, pp. 541-559, 0-87170-804-3.

Samenvatting

Dit werk behandelt een nieuwe fabricagemethode voor microelektronische hotplates. Deze hotplates werken op basis van een klein oppervlak (ter grootte van 0.001^2-0.1^2 mm^2) dat verhit wordt door een verwarmingselement tot 300-400 ºC. Zulke hotplates kunnen worden gebruikt voor bijvoorbeeld gas- of flowsensoren. Bij gebruik als gassensor zal er in aanwezigheid van een brandbaar gas op het (katalytische) oppervlak van de hotplate een verbrandingsreactie optreden waarbij warmte wordt gegenereerd. Deze warmte wordt gedetecteerd via een verandering in de (temperatuurafhanklijke) elektrische weerstand van het verwarmings-element. In een hotplate heeft het verwarmingselement naast hittebron dus ook de functie van temperatuursensor.

Het onderzoek, beschreven in dit werk, maakt deel uit van het 'Hot Silicon' projekt waarin hotplates worden bestudeerd die extreem weinig vermogen (10^{-6} W) gebruiken; een factor 1000 minder dan het vermogen van huidige 'laag vermogen' hotplates. Dit maakt toepassing van hotplates in bijvoorbeeld gassensoren mogelijk in draagbare systemen (op batterijen) in bijvoorbeeld industiële omgevingen of in huis, om daar de aanwezigheid van gevaarlijke (schadelijke en/of brandbare) gassen te meten. Een combinatie van meerdere sensoren ('sensor array') kan worden gebruikt voor de detectie van verschillende gassen. Laag vermogen sensoren zijn in het algemeen veiliger in gebruik.

In dit werk is de hotplate gebaseerd op een kleine hoogohmige geleidende cilinder (de 'link'). Deze is ingebed in een isolerende (glas) laag

en is gepositioneerd tussen twee kruisende elektroden. Het maken van deze cilinder is gebaseerd op het etsen van een gaatje in de glaslaag tussen de twee elektroden. Dit gaatje wordt gecoat met een ultradunne laag (7-15 nm) titaan nitride (TiN). De TiN laag wordt gedeponeerd via atomic layer depositie (ALD). Dankzij de goede stapbedekking van het ALD proces ontstaat in het gaatje een perfecte holle en geleidende cilinder.

In het eerste deel van dit werk zijn de materiaaleigenschappen van dunne ALD TiN films bestudeerd. In het tweede deel zijn de gerealiseerde devices behandeld, evenals de integratie van ALD TiN in het fabricageproces.

In hoofdstuk 2 zijn de soortelijke weerstand (ρ) en de temperatuur-afhankelijkheid van de weerstand (ofwel de 'temperature coefficient of resistance', TCR) gemeten met behulp van speciale teststructuren. De waarden van ρ en de TCR zijn belangrijke parameters voor het ontwerp van de hotplate omdat hiermee de temperatuur van het hete oppervlak nauwkeurig bepaald kan worden. Er is een verband gevonden tussen enerzijds de laagdikte en de soortelijke weerstand en anderzijds tussen soortelijke weerstand en de TCR: dunnere TiN lagen hebben een hogere ρ en TiN lagen met een hogere ρ hebben een lagere TCR. Daarnaast is vastgesteld dat de waardes van de TCR, gemeten tussen de 25 en 175 °C, gelijk blijft tot 600 °C.

In hoofdstuk 3 is het oxidatiegedrag onderzocht van dunne TiN lagen. Gedurende het fabricageproces en tijdens gebruik van de hotplate mag de ALD TiN laag niet oxideren omdat hierdoor de elektrische eigenschappen van de link veranderen. Hoewel TiN als zeer oxidatiebestendig wordt beschouwd, blijkt er weinig voor nodig om 7-15 nm TiN thermisch te oxideren in droge (O_2) en natte (H_2O) atmosfeer op temperaturen van 300 tot 500 °C of tijdens blootstelling aan zuurstof bevattende plasma's. De kinetiek van het oxidatieproces is bestudeerd. De samenstelling van ALD TiN en het

gevormde TiO_2 is vergelijkbaar met die van gesputterde stoichiometrische TiN lagen. Daarnaast is de functionaliteit van diverse beschermlagen getest en het is gebleken dat met behulp van de juiste beschermlaag oxidatie van ultradunne TiN lagen effectief kan worden voorkomen.

In hoofdstuk 4 zijn het ontwerp, het nieuwe fabricageproces en de elektrische karakerisatie van de op de link gebaseerde microelektronische hotplates gepresenteerd. Er zijn hotplates gemaakt met links van verschillende grootte: microlinks (∅ 2-6 μm) en nanolinks (∅100 nm) en bij sommige hotplates is het silicium onder het device weggeëtst. Hierdoor ontstaat een membraan voor thermische isolatie. De microlink hotplates hebben een laagohmige link. Ze bereiken een temperatuur van 250 °C met een vermogen van een 2.7 mW en worden niet warm zonder vrijgeëtst membraan. Bij de nanolink hotplates kan een linktemperatuur worden bereikt van 280 °C met een vermogen van 5.5 μW. Zonder membraan vergt dit slechts een factor 2 meer vermogen. Dit maakt een membraanloze nanolink device een interessante kandidaat voor een mechanisch robuste hotplate.

In hoofdstuk 5 zijn twee technieken onderzocht om de temperatuur te bepalen van de hotplates op een andere manier dan via de temperatuurafhankelijke weerstand van het verwarmingselement. De gebruikte infrarood (IR) thermometrie methode kan goed gebruikt worden voor microlink hotplates. De gebruikte polymeer-smelt-methode kan met succes worden gebruikt voor de temperatuurbepaling van grote ($> 100\times100$ μm^2) oppervlakken. Echter, het is gebleken dat beide methoden, zoals gebruikt in dit proefschrift, niet gevoelig genoeg zijn om geringe warmtegeneratie op het kleine ($< 1\times1$ μm^2) oppervlak in een nanolink hotplate waar te nemen.

Tot slot wordt in hoofdstuk 6 een onverwachte lekstroom door het glas rondom de nanolink (in combinatie met een laag doorslagveld van het glas)

behandeld die optreedt bij sommige hotplates. Deze hoge lekstroom is gerelateerd aan een fundamentele eigenschap van het ALD TiN proces, nodig voor het vormen van de link. De goede stapbedekking heeft hier als nadeel dat de gevoeligheid voor proces gerelateerde fouten in het device enorm wordt versterkt. Structurele defecten in de isolerende glaslaag worden ook opgevuld met geleidend TiN en leiden snel tot een verlaagde doorslagspanning en een laagohmig elektrisch geleidend pad parallel aan de link. Experimenten met gebruik van gesputterde TiN lagen met een mindere stapbedekking laten zien dat deze structurele defecten anders onopgemerkt zouden blijven. Deze experimenten laten duidelijk het belang zien van procesintegratie bij de introductie van nieuwe processtappen en/of materialen.

Summary

In this work, a new fabrication process is investigated for ultralow power, microelectronic hotplates. These hotplates are based on a small surface (0.001^2-0.1^2 mm^2) that is heated by a heater to temperatures in the range of 300-400 °C. These hotplates can be used for instance as gas or flow sensors. Applied as gas sensor, an (exothermic) combustion reaction will take place at the (catalytic) surface in the presence of a flammable gas during which heat is generated. This reaction heat is detected by a change in the (temperature dependent) heater resistance. This means that in a hotplate the heater simultaneously acts as a heat source and thermal sensor.

The research, discussed in this work, is part of the 'Hot Silicon' project in which ultralow power (10^{-6} W) hotplates are studied; the power consumption is a factor 1000 less than state-of-the-art 'low power' heaters. The ultralow power enables integration of hotplates as for instance gas sensors in portable (battery powered) systems for industrial or domestic applications, for instance for the detection of hazardous (harmful and/or flammable) gases. A combination of various sensors (in a 'sensor array' for instance) can be used for the detection of multiple gases. Furthermore, low power gas sensors are generally safer.

In this work, the hotplate is based on a small high ohmic conducting cylinder (the 'link'). The link is embedded in an insulating (glass) layer and positioned between two crossing electrodes. Fabrication of the link is based on etching a hole in the glass layer and coating it with an ultrathin (7-15 nm) titanium nitride (TiN). Due to the excellent step coverage of the ALD process, a perfectly hollow and conducting cylinder is created.

In the first part of this work, the material properties of ALD TiN thin films are studied. In the second part, the realized hotplates are discussed, as well as the integration of ALD TiN in the fabrication process.

In chapter 2, the resistivity (ρ) and the temperature dependence of the resistance (i.e. the temperature coefficient of resistance, TCR) of ultrathin ALD TiN films are measured using special test structures. The values of ρ and TiN are important parameters for the sensor design, as they can be used for an accurate temperature measurement of the hot surface. A relation is established between the TiN layer thickness and the resistivity and between the TCR and the resistivity: thin TiN layers have a higher ρ and TiN with a high resistivity have a lower TCR. Furthermore, it is shown that the TCR, measured between 25 and 175 °C, remains constant up to 600 °C.

In chapter 3, the oxidation behaviour of thin TiN layers is investigated. During the fabrication process and operation hotplate, the ALD TiN layer should not oxidize. Despite the fact that TiN is considered as a very oxidation-proof material, little oxidation is necessary to modify the properties of a 7-15 nm thin film significantly in dry (O_2) and wet (H_2O) atmosphere at temperatures between 300 and 500 °C and during exposure to oxygen containing plasmas. The kinetics of the oxidation process have been studied. The composition of the ALD TiN film and the generated TiO_2 is comparable to sputtered stoichiometric TiN layers. Using a suitable protection layer, the oxidation of ultrathin TiN layers can be prevented effectively.

In chapter 4, the design, the novel fabrication process and the electrical characterization of link-based microelectronic hotplates are shown. Hotplates were fabricated with different link sizes: microlinks (∅ 2-6 µm) and nanolinks (∅ 100 nm) and for some hotplates, the silicon underneath the device is removed. By doing so, a suspended membrane is released for

thermal insulation. Microlink-based hotplates have a low ohmic link. They reach a temperature of 250 °C with a power dissipation of 2.7 mW and cannot be heated without a suspended membrane. Nanolink-based hotplates can reach a temperature of 280 °C with a power consumption of 5.5 μW. Without a suspended membrane, only factor 2 more power is required for the same temperature. This makes a nanolink-based device without a suspended membrane and interesting candidate for a mechanically robust hotplate.

In chapter 5, two techniques are investigated for measuring the temperature of a device using an alternative method than the temperature dependent resistance of the heater. The employed infrared (IR) thermometry method can be applied successfully to microlink-based hotplates. The employed polymer melting method can be applied successfully to measuring large (> 100×100 μm^2) areas. However, it turned out that both methods, as employed in this work, are not sensitive enough to detect the small amount of heat that is generated by the small (< 1×1 μm^2) surface of the nanolink-based hotplates.

Finally, in chapter 6, the unexpectedly high leakage current through the glass around the nanolink is discussed (together with a low breakdown field of the glass) that is observed for some hotplates. The high leakage current is related to a fundamental property of the ALD TiN process, required for manufacturing of the link. The excellent step coverage has the disadvantage that the sensitivity for process related errors in the device increases dramatically. Structural defects in the insulating glass layer are filled in with conducting TiN, leading to a low ohmic conducting path parallel to the link. Experiments using sputtered TiN layers with a worse step coverage show that these structural defects remain unnoticed otherwise. These experiments show the importance of the process integration for the introduction of new process steps and/or materials.

"Ik zou het nog sterker kunnen vertellen,
maar dan moet ik liegen…"

Uit het geheugen van RobW

List of publications

Journal papers

- H. van Bui, **A.W. Groenland**, A. A. I. Aarnink, R. Wolters, J. Schmitz, and A. Y. Kovalgin, ***"Growth Kinetics and Oxidation Mechanism of ALD TiN Thin Films Monitored by In Situ Spectroscopic Ellipsometry",*** Journal of the Electrochemical Society, vol. 153, pp. 214-220, 2010
- **A.W. Groenland**, R.A.M. Wolters, A.Y. Kovalgin, and J. Schmitz, ***"Four point probe structures with buried and surface electrodes for the electrical characterization of ultrathin conducting films",*** IEEE Transactions on Semiconductor Manufacturing *(accepted)*, 2011
- R.M. Tiggelaar, R.G.P. Sanders, **A.W. Groenland**, and J.G.E. Gardeniers, ***"Stability of thin platinum films implemented in high-temperature microdevices",*** Sensors and Actuators A: Physical, vol. 152, pp. 39-47, 2009
- R.M. Tiggelaar, **A.W. Groenland**, R.G.P. Sanders, and J.G.E. Gardeniers, ***"Electrical properties of low pressure chemical vapor deposited silicon nitride thin films for temperatures up to 650 °C",*** Journal of Applied Physics, vol. 105, pp. 033714-6, 2009
- A. Agiral, **A.W. Groenland**, J.K. Chinthaginjala, K. Seshan, L. Lefferts, and J. G. E. H. Gardeniers, ***"On-chip microplasma reactors using carbon nanofibres and tungsten oxide nanowires as electrodes",*** Journal of Physics D: Applied Physics, vol. 41, pp. 194009, 2008
- P.K. Hurley, K. Cherkaoui, S. McDonnell, G. Hughes, and **A.W. Groenland**, ***"Characterisation and passivation of interface defects in (1 0 0)-Si/SiO_2/HfO_2/TiN gate stacks",*** Microelectronics Reliability, vol. 47, pp. 1195-1201, 2007

Conference proceedings / talks / posters

- **A.W. Groenland**, R.A.M. Wolters, A.Y. Kovalgin, and J. Schmitz, ***"A difference in using ALD or PVD TiN as electrode material in MIM and MIS capacitors",*** *(accepted as oral presentation)*, Proceedings of the EuroCVD 18, 2011 *(submitted)*

- **A.W. Groenland**, R.A.M. Wolters, A.Y. Kovalgin, and J. Schmitz, ***"Nano-link based ultra low power micro electronic hotplates for sensors and actuators"*** *(oral presentation)*", ECS transactions, vol. 35, 2011 *(submitted)*
- **A.W. Groenland**, R.A.M. Wolters, A.Y. Kovalgin, and J. Schmitz, ***"Four point probe structures with buried electrodes for the electrical characterization of ultrathin conducting films",*** Proceedings of the IEEE International Conference on Microelectronic Test Structures, Oxnard, USA, 2009, pp 191-195, **(BEST PAPER AWARD)**
- I. Brunets, **A.W. Groenland**, A. Boogaard, T. Aarnink, and A.Y. Kovalgin, ***"A study of thermal oxidation and plasma-enhanced oxidation/reduction of ALD TiN layers",*** *(poster)* Proceedings of the 18th International Conference on Atomic Layer Deposition ALD 2008, Bruges, Belgium, 2008, P54
- P.K. Hurley, K. Cherkaoui, and **A. Groenland**, ***"Electrically Active Interface Defects in the (100)Si/SiOx/HfO2/TiN System: Origin, Instabilities and Passivation",*** ECS Transactions, vol. 3, pp 97-110, 2006

Workshops / non peer reviewed work

- **A.W. Groenland**, R.A.M. Wolters, A.Y. Kovalgin, and J. Schmitz, ***"On the leakage problem of MIM capacitors due to improper etching of titanium nitride",*** in Proceedings of the 13th Annual Workshop on Semiconductor Advances for Future Electronics and Sensors (SAFE), 29-30 Nov 2007, Veldhoven, The Netherlands., pp 89-92
- **A.W.Groenland**, R.A.M. Wolters, A.Y. Kovalgin, and J. Schmitz, ***"Ultra low power detection of flamable gases", (****poster)* STW Annual congress, 7 Oct 2010, Nieuwegein, The Netherlands
- **A.W. Groenland**, R.A.M. Wolters, A.Y. Kovalgin, and J. Schmitz, ***"Contact chain measurements for ultrathin conducting films",*** in Proceedings of the 12th Annual Workshop on Semiconductor Advances for Future Electronics and Sensors, 26-27 Nov 2009, Veldhoven, The Netherlands, pp 150-152
- **A.W. Groenland**, I. Brunets, A. Boogaard, A.A.I. Aarnink, and A. Y. Kovalgin, ***"Thermal and plasma-enhanced oxidation of ALD TiN",*** in Proceedings of the 11th annual workshop on semiconductor advances for future electronics and sensors (SAFE 2008), 27-28 Nov 2008, Veldhoven, The Netherlands, pp 468-471
- A. Agiral, **A.W. Groenland**, J.K. Chinthaginjala, K. Seshan, L. Lefferts, and J.G.E. Gardeniers, ***"On-chip microplasma reactors utilizing tungsten nanowires and carbon nanofibres as electrodes***", (oral presentation) 4th International Workshop on Microplasmas, Tainan, Taiwan, 2007
- **A.W. Groenland**, A.Y. Kovalgin, J. Schmitz, and J. Holleman, "***Simulation of a Nanolink Hot-Plate Device",*** in Proceedings of the 10th Annual Workshop on Semiconductor Advances for Future Electronics and Sensors (SAFE), 29-30 Nov 2007, Veldhoven, The Netherlands. pp. 581-583

Author biography

Alfons W. Groenland was born in Hengelo (ov), The Netherlands, on November 3, 1982. He received his B.Sc. and M.Sc. (*cum laude*) in Electrical Engineering from the University of Twente, Enschede, The Netherlands, in 2005 and 2006, respectively. From 2006 to 2011 he was employed by the MESA+ Institute of Nanotechnology, chair of Semiconductor Components, University of Twente. In his research, under supervision of Prof. R.A.M. Wolters, he worked on nanoscale thermal sensors and actuators for chemical sensor and microreactor applications, with the focus on process integration and device characterization. This thesis is the result of the research carried out during that period. In 2009, he received the Best Paper Award for his contribution to the IEEE ICMTS conference.

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[1, 2] Promotieregelement Universiteit Twente, februari 2007, artikelen 2.4b en 6

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Alfons Groenland, Enschede, 13 juni 2011